



CORTINA

Product Brief

Cortina Systems® CS5333 OC-48 Multi Service Traffic Manager and SAR

Overview

The Cortina Systems® CS5333 is a single chip solution for implementing ATM or Packet Traffic Management, Switching and ATM Segmentation and Reassembly (SAR). The novel, high performance, scalable chip architecture of the CS5333 with its built in ATM AAL5 SAR can aggregate, switch and traffic manage any traffic type (IP, MPLS or ATM) on any port, at OC-48 full duplex performance, enabling OEMs to simplify system design, development and integration. The CS5333 integrates three critical functions into a single chip: simultaneous packet and ATM switching, ultra accurate shaping and scheduling of both Layer 3 IP and Layer 2 ATM traffic, and IP-to-ATM or Frame Relay-to-ATM interworking via an integrated, wire-speed SAR engine.

Features

Introduction

- 1 M Simultaneously Queued and Scheduled Virtual Connections (VCs)
- ATM VC/VP Switching, Queuing and Traffic Management
- Integrated ATM AAL5 SAR and MPLS Switch
- Flexible Congestion and Buffer Management Schemes
- TM 4.1 Compliant, High-Precision Single / Dual Leaky Bucket Policing and Shaping
- Flow Aggregation, Tunneling and Multicast Features
- Extensive Per VC and Per Port Statistics
- Fully Tested Software Development Kit Includes Software Driver Supporting 2 Layers of Abstracted API Functions

Multi-Service Internetworking

- ATM NNI/UNI Look Up, Header Translation and Switching
- MPLS Lookup and Switching
- Pre-Classified IP Datagram Processing for SAR
- Packet and Cell-Based Scheduling and Statistics

Traffic Shaping/Policing

- ATM Forum Traffic Shaping and Policing Algorithms
- 32 K Traffic Shaping and Policing Resources
- Ultra Accurate: Shapes/Policies from 48 Kbps to Line Rate in 1 Cell Increments
- Four Shaping Timing Wheels to Support Real Time and Best Effort Traffic Characteristics and to Elegantly Handle Oversubscription

On-Chip ATM OAM Processing

- Compliant F4/F5 Fault Management OAM Processing
- OAM AIS, RDI, CC, Loopback Request and Reply Generation and Processing
- Checks and Inserts CRC-10
- Inserts and Retrieves OAM Cells from the Data-Path for the Local CPU Processor

QoS Scheduling

- 8 Configurable QoS Classes Per Port or Virtual Output Queue
- CBR, VBRrt, VBRnrt, UBR, UBR+ and GFR Classes of Service
- Strict Priority, Round Robin, Deficit Round Robin, Modified Deficit Round Robin or the Combination Thereof
- Hierarchical Layer 2 and Layer 3 QoS Scheduling

Congestion Management

- Highly Configurable WRED Engine
- Packet-Aware Drops (EPD/PPD)
- Multi-Stage Buffer Management Schemes
- In-Band Flow Control and Back Pressure Mechanisms Across the Data Interfaces

Interfaces

- Two Full-Duplex Data Path Interfaces
 - POS-PHY Level 3 PHY, 32-Bit, 120 Mhz, LVTTTL
 - POS-PHY Level 3 Link, 32-Bit, 120 Mhz, LVTTTL
- Industry Standard External Memory Interfaces
- Generic 32-Bit CPU Interface that Supports Big and Little Endian Processors
- JTAG Port for Boundary Scan and Board Testing

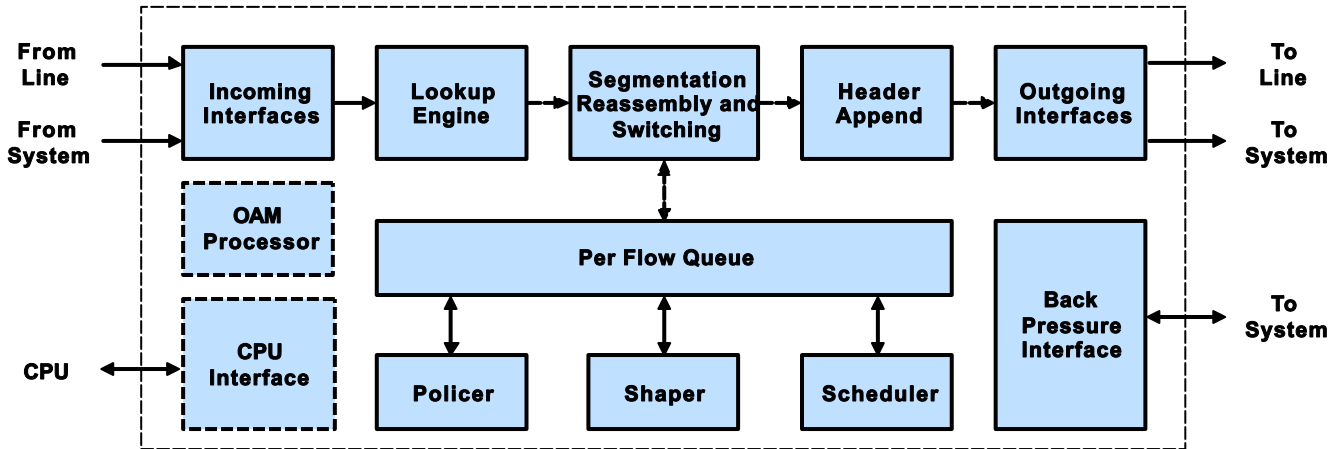
Packaging and Power

- 40 mm x 40 mm Flip Chip BGA
- Low Power: Approximately 5 Watts

Applications

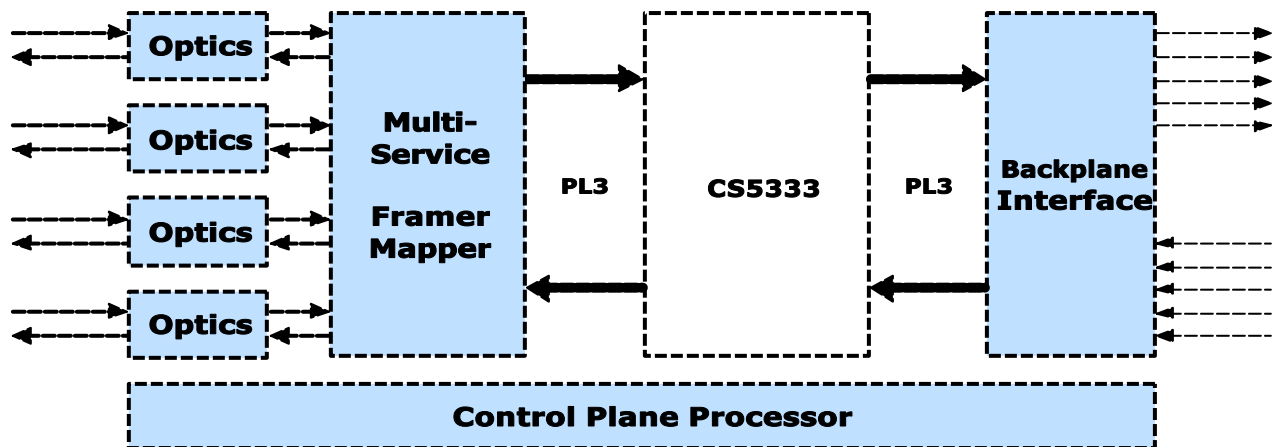
- Edge and Core IP Routers
- Edge and Core ATM/Packet Switches
- Multi-Service / MPLS Switching Platforms
- Broadband Access Multiplexers (DSLAM, PON OLT, CMTS, Wireless Base Stations)

CS5333 Block Diagram



CS5333 Technology

The CS5333 device provides a comprehensive single chip solution for implementing simultaneous Layer 2 and Layer 3 Traffic Management functions including Switching, Queuing and Scheduling. The CS5333 is architected to be both a packet and cell aware device that can switch and manage traffic for both fixed size cells and variable size packets and inter-work transparently between them. The built in line rate AAL5 SAR and OAM processor combined with ATM and MPLS protocol awareness, makes the CS5333 an ideal ATM-Packet Interworking device. The ultra accurate Shaping and Scheduling algorithms of the CS5333 support all the ATM TM 4.1 and DiffServ defined Classes of Services.



Cortina Enables Advanced Services

The CS5333 performs the fine-grained traffic management necessary to deliver carrier class services on as many as 1 M active flows or VCs. Traffic management functions such as Policing, Shaping, Scheduling and Congestion Management features such as buffer management and WRED can be applied to individual flows or an aggregate of flows without affecting the line rate data forwarding performance. The CS5333 also offers built in hardware implemented and software configurable ATM F4/F5 OAM processor.

To support true carrier class Service Level Agreements (SLAs), the CS5333 ATM Switch-SAR collects and stores in external memory a multitude of statistics, both on a per flow as well as on a per interface basis.

The CS5333 device's industry standard interfaces, highly configurable header options, built in flow control and backpressure mechanisms enable ease of integration to other industry standard external devices.

Complete Solution

Cortina provides a complete software development environment that includes a compact PCI based evaluation board system and fully tested software driver with multiple layers of API functions. Cortina's configurable, high-performance, hardware-based ATM Switch and SAR, combined with the proven software driver, enables fast time-to-market for multi-service line card solutions.

Cortina in Communications

Cortina is a leading supplier of intelligent communication solutions through continuous innovations in advanced port processing and intelligent port connectivity to the Core, Metro, Access and Enterprise Market Segments. With our state-of-the-art high speed analog digital integration, we deliver a wide suite of products that address our customers'

performance, density and flexibility needs enabling faster time-to-market, longer time-in-market, and increased revenue opportunities. Working closely with our customers to understand their system requirements and anticipate their needs, we are creating the foundation ingredients for new generations of services.

*Other names and brands may be claimed as the property of others.



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