



Cortina Systems® IXF1110 1000 Mbps Ethernet Media Access Controller

Errata

13 April 2009

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Revision 12.0

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Revision History

Revision 12.0 Revision Date: 13 April 2009
Four new Specification Changes have been added (Item #1 on page 13 through Item #4 on page 13). These Specification Changes have been updated in the Cortina Systems® IXF1110 1000 Mbps Ethernet Media Access Controller Datasheet, document number 250210, revision 11.0.
Revision Number: 11.0 Revision Date: 8 September 2007
Added Erratum 13 ; <i>Undercounting and Missed Status of Clear on Read Registers</i>
Revision Number: 10.0 Revision Date: 5 July 2007
<ul style="list-style-type: none">• First release from Cortina Systems, Inc.• Added Erratum 11; <i>Reduction in CLK50 Range of Operation</i>• Added Erratum 12; <i>Voltages for CLK125 and CLK50 Incorrect</i>• Added Item 5; <i>RxSymbolError Counter Clarification</i>
Revision Number: 009 Revision Date: 14-Oct-2005
<ul style="list-style-type: none">• Replaced Marking diagram under “Identification Information”.• Added RoHS compliant part number in Table 2, “Product Information” on page 21 and modified Figure 2, “Ordering Information - Sample” on page 21 under “Documentation Changes”.
Revision Number: 008 Revision Date: August 31, 2004
<ul style="list-style-type: none">• Removed old Item 1: SPI4-2 Interface Signal Descriptions Table from “Documentation Changes” table.• Corrected table number from 105 to 98 under “TX FIFO Drain Register (\$0x620) (Section 8.5.6: TX Block Register Overview of the IXF1110 MAC Datasheet)” under “Specification Clarifications”.• Removed old Item 1: SPI4-2 Interface Signal Descriptions Table from “Documentation Changes” section.
Revision Number: 007 Revision Date: July 27, 2004
<ul style="list-style-type: none">• Corrected Signal names to AVDD2P5_1 and AVDD1P8_2 in “Documentation Changes”.• Corrected Signal name to AVDD2P5_1 in “Documentation Changes”.
Revision Number: 006 Revision Date: June 30, 2004
<ul style="list-style-type: none">• Add Item 10: “Forced Mode Operation” to the “Errata” table.• Moved items 1,2, and 5 in the “Specification Changes” table to the “Specification Clarifications” table.• Deleted items 3 and 4 from the “Specification Changes” table.• Added Item 10: “Forced Mode Operation” to the “Errata” section.• Moved items 1,2, and 5 in the “Specification Changes” section to the “Specification Clarifications” section and modified descriptions.

Revision Number: 005
Revision Date: March 24, 2004

- Added Stepping 2 to “[Errata](#)” table; changed status of Errata Nos. 2, 3, 5, 6, 7, 8, and 9 from “PlanFix” to “Fixed.”
- Modified diagram under “[Identification Information](#)”
- Modified Stepping/Revision Numbers table under “[Identification Information](#)” [Added Stepping 2 {B2}; changed “Part Number” to “Version ID Number” and added version IDs for Steppings 1 and 2; added table note 1.
- Changed Erratum 2, “[DIP2 Err Counter Cleared Upon Reading SPI4-2 Registers](#)” from “This erratum may be fixed in a future stepping of the product” to “This erratum has been previously fixed.”
- Changed Erratum 3, “[TSCLK Not Output At a Low Voltage](#)” from “This erratum may be fixed in a future stepping of the product” to “This erratum has been previously fixed”; deleted note.
- Changed Erratum 5, “[RX FIFO Overflow May Cause An Out-of-Sequence Event](#)” from “This erratum may be fixed in a future stepping of the product” to “This erratum has been previously fixed.”
- Changed Erratum 6, “[RX FIFO Overflow May Cause a Packet With All Zeros and a Missing EOP on the SPI4-2 Interface](#)” from “This erratum may be fixed in a future stepping of the product” to “This erratum has been previously fixed.”
- Changed Erratum 7, “[RX FIFO Overflow May Cause SOPs Within Eight Cycles on the SPI4-2 Interface](#)” from “This erratum may be fixed in a future stepping of the product” to “This erratum has been previously fixed.”
- Changed Erratum 8, “[EOP Abort Packets Under 80 Bytes May Be Dropped by the IXF1110 TX FIFO](#)” from “This erratum may be fixed in a future stepping of the product” to “This erratum has been previously fixed.”
- Changed Erratum 9, “[RX SPI4-2 Transmission Between Ports 0 and 1 is Unbalanced](#)” from “This erratum may be fixed in a future stepping of the product” to “This erratum has been previously fixed.”
- Added Items 1 through 5 under “[Specification Changes](#)”.
- Added B2 information to “[Product Ordering Information](#)”.

Revision Number: 004
Revision Date: December 8, 2003

- Added Errata 1 through 9 to “[Errata](#)” table.
- Modified diagram under “[Markings](#)”.
- Added Errata 1 through 9 to “[Errata](#)” section.
- Rolled information under “[Documentation Changes](#)” section into Revision 005 of the IXF1110 MAC Datasheet and deleted from this document.

Revision Number: 003
Revision Date: July 22, 2003

Initial customer release.

1.0 Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

1.1 Affected Documents/Related Documents

Title	Document Number
Cortina Systems® IXF1110 1000 Mbps Ethernet Media Access Controller Datasheet	250210

1.2 Nomenclature

Errata are design defects or errors. These may cause the Cortina Systems® IXF1110 1000 Mbps Ethernet Media Access Controller (IXF1110 MAC) behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

2.0 Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the IXF1110 MAC product. Cortina Systems, Inc. (Cortina) may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

2.1 Codes Used in Summary Table

2.1.1 Stepping

X: Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.

(No mark)

or (Blank box): This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

2.1.2 Page

(Page): Page location of item in this document.

2.1.3 Status

Doc: Document change or update will be implemented.

PossibleFix: This erratum may be fixed in a future stepping of the product.

Fixed: This erratum has been previously fixed.

NoFix: There are no plans to fix this erratum.

2.2 Errata (Sheet 1 of 2)

No.	Steppings		Page	Status	Errata
	#1	#2			
1	X	X	page 9	NoFix	73-Byte TX SPI4-2 EOP Abort Packet Counted As a Good Packet
2	X		page 9	Fixed in Rev 2	DIP2 Err Counter Cleared Upon Reading SPI4-2 Registers
3	X		page 9	Fixed in Rev 2	TSCLK Not Output At a Low Voltage
4	X	X	page 9	NoFix	Transition Directly from SATISFIED to STARVING State on RX SPI4-2 Status Bus Input May Result in a Burst Size of Maxburst2 Instead of MaxBurst1
5	X		page 10	Fixed in Rev 2	RX FIFO Overflow May Cause An Out-of-Sequence Event
6	X		page 10	Fixed in Rev 2	RX FIFO Overflow May Cause a Packet With All Zeros and a Missing EOP on the SPI4-2 Interface
7	X		page 10	Fixed in Rev 2	RX FIFO Overflow May Cause SOPs Within Eight Cycles on the SPI4-2 Interface
8	X		page 10	Fixed in Rev 2	EOP Abort Packets Under 80 Bytes May Be Dropped by the IXF1110 MAC TX FIFO

2.2 Errata (Sheet 2 of 2)

No.	Steppings		Page	Status	Errata
	#1	#2			
9	X		page 11	Fixed in Rev 2	<i>RX SPI4-2 Transmission Between Ports 0 and 1 is Unbalanced</i>
10	X		page 11	Fixed in Rev 2	<i>Forced Mode Operation</i>
11	X	X	page 11	NoFix	<i>Reduction in CLK50 Range of Operation</i>
12	X	X	page 11	Fixed in Rev 2	<i>Voltages for CLK125 and CLK50 Incorrect</i>
13	X	X	page 11	NoFix	<i>Undercounting and Missed Status of Clear on Read Registers</i>

2.3 Specification Changes

No.	Steppings		Page	Specification Changes
	#1	#2		
1	X	X	page 13	<i>Add a 10/100 MHz Ferrite Bead across the Resistor on the Analog Power Supply Filter Network</i>
2	X	X	page 13	<i>The 3.3 V Input Signals in the DC Specifications Table have Been Changed</i>
3	X	X	page 13	<i>Updated Values in the LED Interface AC Timing Parameters Table</i>
4	X	X	page 13	<i>LVTTTL Overshoot Limits Have Been Changed</i>

2.4 Specification Clarifications

No.	Steppings		Page	Specification Clarifications
	#1	#2		
1	X		page 14	<i>TX FIFO Drain (Section 6.3.1.3 of the IXF1110 MAC Datasheet)</i>
2	X		page 14	<i>Pause Packets Drop Enable Behavior Table (Section 5.1.2.3.5: Filter PAUSE Packets of the IXF1110 MAC Datasheet)</i>
3	X		page 14	<i>TX FIFO Drain Register (\$0x620) (Section 8.5.6: TX Block Register Overview of the IXF1110 MAC Datasheet)</i>
4	X	X	page 15	<i>CALENDAR_M</i>
5	X	X	page 15	<i>RxSymbolError Counter Clarification</i>

3.0 Errata

Erratum 1: 73-Byte TX SPI4-2 EOP Abort Packet Counted As a Good Packet

Problem If a 73-byte EOP abort packet with a valid CRC is received on the TX SPI4-2 interface, the packet is counted as a good packet by the IXF1110 MAC Statistics, not as a CRC error. The packet is still sent out of the MAC the same as all EOP abort packets, with the CRC invalidated. This only occurs if the CRC append bit in the Diverse Config Register (\$Port_Index + 0x18) is not set.

Implication If a 73-byte EOP abort packet is sent to the IXF1110 MAC TX SPI4-2 interface, the packet is counted as good. However, the packet is still treated the same as any other EOP abort packet.

Workaround Set the CRC append bit in the Diverse Config Register (\$Port_Index + 0x18).

Status NoFix

Erratum 2: DIP2 Err Counter Cleared Upon Reading SPI4-2 Registers

Problem The Dip2 error bit (bit 20 in the SPI4-2 RX Calendar Register [\$0x702]) can be cleared if any SPI4-2 Registers (\$ 0x700, 0x701, or 0x703) are read.

Implication If the SPI4-2 RX Calendar Register (\$0x702) is not read before the SPI4-2 Registers (\$ 0x700, 0x701, 0x703), the DIP 2 err bit may be cleared and undetected by system software.

Workaround When reading the SPI4-2 Register block (\$ 0x700-0x704), the SPI4-2 RX Calendar Register (\$0x702) must be read first to properly detect DIP2 errors.

Status Fixed in Rev 2

Erratum 3: TSCLK Not Output At a Low Voltage

Problem When VDD (1.8 V) is operating at 1.71 V, the TSCLK may not output even though a valid TDCLK is applied.

Implication The TSCLK may not be output when operating at a low voltage. Therefore, data transmissions on the TX SPI4-2 may not be possible until the clock is output.

Workaround None.

Status Fixed in Rev 2

Erratum 4: Transition Directly from SATISFIED to STARVING State on RX SPI4-2 Status Bus Input May Result in a Burst Size of Maxburst2 Instead of MaxBurst1

Problem If the RX FIFO status bus from the NPU or SPI4-2 ASIC transitions directly from SATISFIED to STARVING for a given port, a burst the size of Maxburst2 may be sent.

Implication STARVING status should result in an RX SPI4-2 data burst of the size programmed into Maxburst1 (MB1). If the RX Status bus transitions directly from STARVING to SATISFIED while the IXF1110 MAC is scheduled to send this MB1 size burst, a shorter burst of MB2 size may be sent. No data loss or packet corruption occurs from the shorter burst. The balance of the packet data is sent once the Status bus transitions out of the SATISFIED state.

Workaround None.

Status NoFix

Erratum 5: RX FIFO Overflow May Cause An Out-of-Sequence Event

Problem When the RX FIFO on the IXF1110 MAC overflows, a SPI4-2 out-of-sequence event for that port may occur. The following is an example of what may be seen:

SOP
Data(xN)
EOP -- Good termination
Idle(xN) -- Numerous idles may occur.
Data continuation word – Out-of-sequence control word – no SOP
Data(xN) -- Only one data word occurs
EOP Abort
Idle – Numerous idles may occur
SOP – Start of the next packet
Data(xN)
EOP

Implication When an RX FIFO overflow occurs, an out-of-sequence SPI4-2 event can occur. The upstream SPI4-2 device may receive an out-of-sequence event from the IXF1110 MAC. This erratum does not occur if the RX FIFO does not overflow.

Workaround None.

Status Fixed in Rev 2

Erratum 6: RX FIFO Overflow May Cause a Packet With All Zeros and a Missing EOP on the SPI4-2 Interface

Problem A packet may be output with all zeros with a missing EOP when the IXF1110 MAC RX FIFO overflows.

Implication An out-of-sequence SPI4-2 event can occur when an RX FIFO overflow occurs. The attached SPI4-2 device could receive an out-of-sequence event from the IXF1110 MAC. This errata does not occur if the RX FIFO does not overflow.

Workaround None.

Status Fixed in Rev 2

Erratum 7: RX FIFO Overflow May Cause SOPs Within Eight Cycles on the SPI4-2 Interface

Problem Two SOPs may be output less than eight cycles apart when the RX FIFO overflows.

Implication When an RX FIFO overflows, two SOPs less than eight cycles apart may occur on the RX SPI4-2 interface. This errata does not occur if the RX FIFO does not overflow.

Workaround None.

Status Fixed in Rev 2

Erratum 8: EOP Abort Packets Under 80 Bytes May Be Dropped by the IXF1110 MAC TX FIFO

Problem One of the EOP abort packets may be dropped if consecutive EOP abort packets are received within 6-7 idles on the TX SPI4-2.

Implication Consecutive SPI4-2 EOP abort packets under 80 bytes may result in one of the EOP abort packets being dropped and not sent out from the SerDes interface.

Workaround None.

Status Fixed in Rev 2

Erratum 9: RX SPI4-2 Transmission Between Ports 0 and 1 is Unbalanced

Problem When only ports 0 and 1 are transmitting data and have data to send to the upstream SPI4-2 device, the order of transfer from these ports may not be even.

Implication Sending data to ports 0 and 1 data transmission out the SPI4-2 may not be evenly weighted.

Workaround None

Status Fixed in Rev 2

Erratum 10: Forced Mode Operation

Problem Ports operating in forced mode out of reset or power-up may be unable to transmit data out of the TX SerDes.

Implication Ports operating in forced mode may indicate synchronization has occurred but will continue to output a SATISFIED status on the SPI4-2 TX FIFO status bus out of reset or power-up.

Workaround After any device reset or power-up, toggle bit 5 “AN_enable” of the Diverse Config Register (\$Port_Index + 0x18) by setting the bit to ‘1’ and then back to ‘0’ for all ports that are to be configured in forced mode. This must be done as part of the initialization sequence after a valid TDCLK is applied and a valid TSCLK is output by the device.

Status Fixed in Rev 2

Erratum 11: Reduction in CLK50 Range of Operation

Problem When the CLK50 clock is running below 42 MHz, the Rx stat counter is unable to run fast enough to keep up with the request for stat updates from the MAC clock domain.

Implication Rx stat counters undercounting packet and octet counts despite no packet errors in IXF1110 MAC.

Workaround Run the CLK50 between 42 MHz and 50 Mhz (old specification is 40 Mhz–50 MHz). The IXF1110 MAC datasheet is updated with new specification.

Status NoFix

Erratum 12: Voltages for CLK125 and CLK50 Incorrect

Problem The voltages for CLK125 and CLK50 were 2.5 V CMOS.

Implication The voltages for CLK125 and CLK50 should be 3.3 V LVTTTL.

Workaround Changed voltages for CLK125 and CLK50 from 2.5 V CMOS to 3.3 V LVTTTL.

Status Fixed in Rev 2

Erratum 13: Undercounting and Missed Status of Clear on Read Registers

Problem The following registers occasionally undercount or miss status under certain conditions:

-
- RX FIFO Number of Frames Removed
 - TX FIFO Number of Frames Removed
 - RX FIFO Overflow EventTX FIFO Overflow Event
 - TX FIFO Info Out-of-Sequence

The first two registers (RX FIFO Number of Frames Removed and TX FIFO Number of Frames Removed) are counters that log the number of frames which have been dropped from an RX FIFO or TX FIFO, respectively.

The remaining three registers (RX FIFO Overflow Event, TX FIFO Overflow Event, and TX FIFO Info Out-of-Sequence) are status registers that set bits whenever the respective condition occurs. These registers will lose increments/status whenever a CPU read and a counter increment request/event occur during the same internal clock cycle. Only the register that is read by the CPU is affected by losing the new counter increment/status. The prior contents of the register will be returned successfully during the CPU read.

Implication Whenever one of the five registers is read, a slight chance exists that an increment or status may be lost if a concurrent update is occurring to the accessed register. For the RX FIFO Number of Frames Removed and TX FIFO Number of Frames Removed counters, an increment might be lost. For the RX FIFO Overflow Event, TX FIFO Overflow Event, and TX FIFO Info Out-of-Sequence registers, status may be lost. From lab observations, the amount of lost increments/status is very small ($\ll 1\%$). The problem is most frequent when the packet rate is high and the register polling interval is small.

Workaround The occurrence can be reduced by increasing the polling interval.

Status NoFix

4.0 Specification Changes

Item 1: Add a 10/100 MHz Ferrite Bead across the Resistor on the Analog Power Supply Filter Network

Description Add a Ferrite Bead (FB) across the resistor to decrease noise and to stabilize the power.

Documents Updated in the Cortina Systems® IXF1110 1000 Mbps Ethernet Media Access Controller Datasheet, revision 11.0, document number 250210

Item 2: The 3.3 V Input Signals in the DC Specifications Table have Been Changed

Description The Input High Voltage (VIH) has changed from a minimum of 1.7 V to a minimum of 2.0 V and the Input Low Voltage (VIL) has changed from a maximum of 0.7 V to a maximum of 0.8 V.

Documents Updated in the Cortina Systems® IXF1110 1000 Mbps Ethernet Media Access Controller Datasheet, revision 11.0, document number 250210

Item 3: Updated Values in the LED Interface AC Timing Parameters Table

The Tdatd, Tlath and Tlatl parameter values and parameter names in the LED Interface AC Timing Parameters table are corrected in the Cortina Systems® IXF1110 1000 Mbps Ethernet Media Access Controller Datasheet, revision 11.0, document number 250210

The parameter values shown in [Table 1](#) have been changed to the values shown in [Table 2](#):

Table 1 Previous LED Interface AC Timing Parameters

Symbol	Parameter	Min	Max	Units
Tdatd	LED_CLK falling edge to LED_DATA valid	2	5	ns
Tlath	LED_CLK rising edge to LED_LATCH rising edge	690	700	µs
Tlatl	LED_CLK falling edge to LED_LATCH falling edge	690	700	µs

Table 2 Corrected LED Interface AC Timing Parameters

Symbol	Parameter	Min	Max	Units
Tdatd	LED_CLK falling edge to LED_DATA valid	–	5	ns
Tlath	LED_CLK falling edge to LED_LATCH rising edge	–	5	ns
Tlatl	LED_CLK rising edge to LED_LATCH falling edge	–	5	ns

Documents Updated in Cortina Systems® IXF1110 1000 Mbps Ethernet Media Access Controller Datasheet, revision 11.0, document number 250210

Item 4: LVTTTL Overshoot Limits Have Been Changed

Description The overshoot limits on 3.3 V LVTTTL pins have been changed from 3.9 V to 5.5 V.

Documents Updated in the Cortina Systems® IXF1110 1000 Mbps Ethernet Media Access Controller Datasheet, revision 11.0, document number 250210

5.0 Specification Clarifications

Item 1: TX FIFO Drain (Section 6.3.1.3 of the IXF1110 MAC Datasheet)

The TX FIFO drain feature applies to Revision 2 only. Prior steppings do not have this feature.

Item 2: Pause Packets Drop Enable Behavior Table (Section 5.1.2.3.5: Filter PAUSE Packets of the IXF1110 MAC Datasheet)

For steppings prior to Revision 2, Pause Frames cannot be filtered when Flow Control is disabled in the FC Enable Register (\$Port_Index + 12).

Item 3: TX FIFO Drain Register (\$0x620) (Section 8.5.6: TX Block Register Overview of the IXF1110 MAC Datasheet)

Status If the **Revision 2** stepping is used, see Table 98: TX FIFO Drain (\$0x620) Register in the IXF1110 MAC Datasheet.

If the **Revision 1** stepping is used, see Table 1 “TX FIFO Port Reset Register (Addr: 0x620)” below.

Table 3 TX FIFO Port Reset Register (Addr: 0x620) (Sheet 1 of 2)

Bit	Name	Description	Type ¹	Default
Register Description: This is a soft reset register for each port in the TX block. Port ID = bit position in the register. To make the reset active, the bit must be set High (for example, reset of port 4 implies register value = 0001.0000, setting the bit to 0 de-asserts the reset).				0x00000000
31:10	Reserved	Reserved	R	0x000000
9	TX FIFO Port 9 Reset	Port 9 0 = De-assert reset 1 = Reset	R/W	0
8	TX FIFO Port 8 Reset	Port 8 0 = De-assert reset 1 = Reset	R/W	0
7	TX FIFO Port 7 Reset	Port 7 0 = De-assert reset 1 = Reset	R/W	0
6	TX FIFO Port 6 Reset	Port 6 0 = De-assert reset 1 = Reset	R/W	0
5	TX FIFO Port 5 Reset	Port 5 0 = De-assert reset 1 = Reset	R/W	0
4	TX FIFO Port 4 Reset	Port 4 0 = De-assert reset 1 = Reset	R/W	0
<ol style="list-style-type: none"> 1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write 2. When performing a tx_fifo_reset during a TX packet transfer, the statistics generated for the aborted packet do not reflect what is currently on the line. Due to the internal alignment of data into 8 byte strips the octet if the reset occurs on the 64 to 65 byte boundary the statistics register could be out by up to 8 bytes. 				

Table 3 TX FIFO Port Reset Register (Addr: 0x620) (Sheet 2 of 2)

Bit	Name	Description	Type ¹	Default
3	TX FIFO Port 3 Reset	Port 3 0 = De-assert reset 1 = Reset	R/W	0
2	TX FIFO Port 2 Reset	Port 2 0 = De-assert reset 1 = Reset	R/W	0
1	TX FIFO Port 1 Reset	Port 1 0 = De-assert reset 1 = Reset	R/W	0
0	TX FIFO Port 0 Reset	Port 0 0 = De-assert reset 1 = Reset	R/W	0

1. R = Read Only; CoR = Clear on Read; W = Write; R/W = Read/Write
2. When performing a tx_fifo_reset during a TX packet transfer, the statistics generated for the aborted packet do not reflect what is currently on the line. Due to the internal alignment of data into 8 byte strips the octet if the reset occurs on the 64 to 65 byte boundary the statistics register could be out by up to 8 bytes.

Item 4: CALENDAR_M

Description CALENDAR_M is the SPI4-2 parameter that specifies the number of times the calendar port status sequence is repeated between the framing and DIP2 cycle of the calendar sequence. The IXF1110 MAC datasheet erroneously reported this parameter as programmable prior to Revision 007.

Status For the IXF1110 MAC, CALENDAR_M is fixed at 1 for the TX Path and RX Path. A calendar of one repetition must be sent on the RX FIFO Status.

Item 5: RxSymbolError Counter Clarification

Description Assumption could be made that the counter would count all symbol errors even if no packet was being received.

Status Added clarification that the counter increments once for each packet that encounters symbol errors during reception. Symbol errors between packets are not counted.



For additional product and ordering information:

www.cortina-systems.com