Cortina Systems® IXF1012 12-Port and IXF1024 24-Port 10/100/1000 Ethernet Media Access Controllers

Frequently Asked Questions

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Contents

Revision History

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1.0 Introduction

This document is a compilation of the most frequently asked questions (FAQs) and corresponding answers for the the Cortina Systems® IXF1012 12-Port and IXF1024 24-Port 10/100/1000 Mbps Ethernet Media Access Controller (MACs). These two devices are collectively referred to as the IXF1012/1024 MAC throughout this document.

2.0 General Questions

Question 1 **What packet filtering methods are supported?**

Answer Registers can be programmed to enable packet filtering for unicast, multicast, VLAN packets and pause packets on a per port basis. All VLAN and Pause packets can be passed or dropped, up to 3 unicast and up to 6 multicast addresses can be programmed to be passed.

Question 2 **What packet classification options are available?**

Answer The following packets can be classified as High or normal priority: Pause, VLAN and up to 6 unique multicast addresses. Eight programmable priority levels total are available within the High and Normal priority FIFOs.

Question 3 **What is the Maximum size packet that can be supported?**

Answer The maximum value that can be loaded into the Max Frame Size register is 10k or 10240 bytes. Received packets that exceed this limit will be truncated and appended with a EOP abort; they may be dropped if the device is programmed to drop bad packets. Transmitted packets that exceed this limit will be truncated and appended with a bad CRC.

Question 4 **What minimum Tx FIFO high watermark value should be used?**

Answer The minimum value is one setting greater than the largest size valid packet that will be transmitted. An EOP must be loaded into the Tx FIFO before the High watermark is reached or the frame will be truncated and appended with a bad CRC.

Question 5 **What is the size of the Tx FIFO?**

Answer The Tx FIFO is approximately 12 k or more specifically 12,032 bytes.

Question 6 **Can the High Priority and Normal Priority watermarks be set independently?**

Answer The RX FIFO watermarks can be set independently, however, the Page Watermarks must be set to the same value.

Question 7 **What is the number of bytes in a Jumbo Frame as mentioned in the datasheet?**

Answer A Jumbo Frame is 9.6 k or 9843 bytes, assuming at most 3 nested VLANs.

Question 8 **What is the minimum IPG supported?**

Answer The transmitter is designed to transmit packets with as little as 6 bytes of IPG. The receiver is designed to tolerate as few as 8 bytes of IPG.

Question 9 **When running data rate tests with the SPI4-2 data looped from the ingress path back to the egress path, why do some packets get lost?**

Answer The behavior is likely due to ppm differences in the data transmission rates between the tester and the MAC. For example if the IXD1024 Evaluation Board transmits data at a line rate of 1.25 GHz (-100ppm) and the tester transmits data to the board at 1.25 GHz (+100ppm), the FIFOs will overflow and data will be lost over time due to over-clocking from the slight difference in rates.

To determine if this is the source of the data loss there are two options:

- Set the MAC TX_IPG to 0x7 instead of 0x08 in the IPG Transmit Time Register, $Port Index + 0x10. The IPG reduction allows the slower clock of the MAC device to keep up with the data input rate.
- Set the tester to 99% line rate to resolve the behavior.

Note: In any design there is always a ppm difference between the Rx and the Tx clocks. If the data is looped back as in a test environment the behavior may be present.

Question 10 **What are the thermal characteristics of the MAC device?**

Answer The thermal characteristics of the MAC device are as follows:

- Operating Conditions:
  - Maximum Case Temperature (TOPC) = 101 °C
  - Maximum Junction Temperature (TOPJ) = 104 °C
- Device Characteristics:
  - Junction-to-Ambient (Theta ja) = 9.2 °C/W
  - Junction-to-Top of package (Psi jt) = 0.6 °C/W
- 2-Resistor Model Values:
  - Junction-to-Case (Theta jc) = 0.39 °C/W
  - Junction-to-Board (Theta jb) = 3.56 °C/W

Note: Maximum case temperature is specified in the associated product datasheet and additional details are provided in the Thermal Design Considerations Application Note, document number 310317).

Question 11 **Are the I/Os 3.3V tolerant?**

Answer The CPU interface can be run from a 3.3 V or 2.5 V supply connected to the MAC device. The other single-ended inputs are supplied from a 2.5 V source on the MAC and are 3.3 V tolerant.

Question 12 **What methods of Flow Control are available on the MAC devices?**

Answer Individual Rx FIFO settings based upon Normal and High Priority FIFOs, Rx FIFO memory page limit, SPI4-2 status, and exclusive of previous methods external control by the SSB interface.

3.0 Schematic Questions

Question 13 **Should TRST_L be pulled High or Low when not used?**

Answer In normal device operation TRST_L should be pulled down with a 10 k Resistor.

Question 14 **What should be done with the LED signals when not used?**

Answer Use 4.7 k resistor pull-downs on the Yellow, Blink and LED_CLK LED inputs.

Question 15 **What is done with unused RGMII ports, for example only 10 ports are required?**

Answer The unused RGMII inputs can be directly tied to ground, they do not have to go through resistors to ground. The outputs can be left unconnected. Unused ports should be left in the default disabled state in the Port Enable Register (address $0x500).

Question 16 **When a design does not require all ports, what ports should be used?**

Answer The optimal configuration is to evenly spread the ports between the three 8 port groups (0-7, 8-15 and 16-23). For example, if 8 ports are implemented using the 12-port MAC device, then ports 1, 3, 5, 9, 11, 13, 17, 19 could be used. If 20 ports are implemented using the 24-port MAC device then ports 0-6, 8-13, and 16-22 could be used.

Question 17 **Are terminations required for the lower address bits A1/A0 for 8-bit, 16-bit or 32-bit data bus applications?**

Answer In 8-bit mode address bits A0 and A1 are used and must be connected to the CPU.

In 16-bit mode the address bit A0 is unused and may be pulled down with a 4.7 k resistor.

In 32-bit mode the address bits A1 and A0 are unused and may be pulled down independently with 4.7 k resistors.

4.0 Register Programming Questions

Question 18 **What register settings are required to use SSB Flow Control, other than enabling the SSB bit in the FC Enable Register $Port_Index + 0x16?**

Answer The following registers settings are required to use SSB Flow Control:

- To enable any of the Flow Control abilities, bit 2:0 of the FC Enable Register ($Port_Index + 0x16) must be properly enabled.
- To ensure the pause SSB interface is the sole source of Pause frame generation, the RX FIFO High Watermarks ($Port Index + 0xA0/0xE0) and RX FIFO Page High Watermarks ($Port Index + 0xA9/0xE9) must be programmed to their maximum value. The maximum value is greater than the number of pages and amount of memory that is available and will prevent the watermarks from being reached and triggering flow control packets.
- The SPI4-2 Flow Control Enable Register ($0x70D) must be disabled to prevent Flow Control frames from being generated by the SPI4-2 interface.
- In addition, Periodic Flow Control and Rate Control must not be enabled. (These features are disabled by default.)

Question 19 **What register settings are required to enable and use the MDC/MDIO interface?**

Answer The MDC clock should be running after reset at 2.5 MHz, the default setting. However, the MDIO signal must be enabled for the MDC/MDIO interface to be functional.

The following programming steps must be completed to use the MDIO interface:

1. Complete other required initializations, leaving the MDIO interface disabled by default.
2. Enable and program interface speed to 2.5 MHz or 18 MHz and enable the MDIO signal with MDIO Control Register: $0x583, bits 2 and 0.
3. For MDIO Writes, write the data for the external PHY write to MDIO Single Read and Write Data Register: $0x581.

   For MDIO Reads, when the access is indicated as complete by bit 20 of $0x580, Register $0x581 should be read to retrieve the requested register data
4. The PHY address, register address, command type (read or write) and command execution (enabling execution of the programmed read or write) must all be programmed. Refer to MDIO Single Command Register: $0x580 for details.
5. The previous programming operations must be complete before the following operation can be programmed and initiated:
   If the IXP425 or IXC1100 processor is used, then the CPU mode bits 6:5 in the CPU Mode Select Register: $0x50C must be set to 11.

Question 20 **What are the registers that are different between the IXF1012 MAC device and the IXF1024 MAC device?**

Answer RSTAT Programmable Calendar Registers, Page 0, 0x000 + Offset:

- 0x40, Calendar Length

Global Status and Configuration Registers, Page 0, 0x500 + Offset:

- 0x00, Port Enable Register

- 0x06, MAC Soft Reset
- 0x1B, Interrupt Group Source
- 0x1F, Priority Mode

SPI4-2 Block Registers, Page 0, 0x700 + Offset:

- 0x02, SPI4-2 Calendar Register
- 0x0D, Flow Control
- 0x0F, Group Fairness Weighting Group 0
- 0x10, Group Fairness Weighting Group 1
- 0x11, Group Fairness Weighting Group 2

Rx High/Normal Priority FIFO Registers, Port Index + Offset:

- 0xA6/E6, Page Controller Mode
- 0xAF/EF, Port Interrupt

Tx FIFO Registers, Port Index + Offset:

- 0xCA, Interrupt Status

5.0 SPI4-2 Interface Questions

Question 21 **What is the worst case delay from all ports RX Satisfied until Rx FIFO ingress traffic stops?**

Answer The worst case time would be the time for one calendar cycle to complete (assuming the Satisfied status is reached just after the port slot is reported to the MAC), plus the time to send one MaxBurst1 across the SPI4-2 interface.

Question 22 **What is the worst case delay from RX starving status to traffic on SPI4-2?**

Answer The timing is worst case based upon one cycle time of the calendar running at 1/4 the SPI4-2 speed for LVTTL status bus and a loading time from when the calendar port entry earns credits until the data starts being driven on the SPI4-2 data bus for that port entry.

The loading time is 38 internal clock periods. The clock periods are SPI4-2 bus speed divided by 2. The internal clock is 50 MHz for quarter-rate operation and 200 MHz for full-rate.

For example, the timing for quarter-rate operation using a 24-entry calendar would be: calendar cycle time + loading time = 1040ns(26*40ns) + 760ns(38*20ns) = 1800 ns.

Note: Calendar cycle time includes DIP2 and Framing)

Question 23 **Does the SPI4-2 interface have internal terminations?**

Answer TDCLK_P/N, TCTL_P/N, and TDAT_P/N are internally terminated with 100 Ω differential.

Question 24 **What is the clock source for the SPI4-2 interface?**

Answer The CLK50 input is multiplied by 8 for the normal mode and by 2 for quarter-rate mode.

Question 25 **Can Dynamic Phase Alignment be disabled?**

Answer No, it is enabled in all normal operating modes.

Question 26 **Does the MAC device support SPI4-2 Slave Mode, where the TDCLK clock can be used to source the RDCLK internal to the device?**

Answer This mode is not supported.

Question 27 **What is the allowable frequency difference between SPI4-2 partners, for example the egress path device clock driving the MAC and the MAC SPI4-2 internal frequency?**

Answer The maximum difference between clocks is the maximum frequency range for the MAC. For example, one device can run its SPI4-2 interface at 315 MHz and the other at 400 MHz.

Question 28 **How can less than 24 ports be implemented using 16-Entry Calendar mode?**

Answer The 16-Entry Calendar Mode is designed to support 24 MAC ports using 16 SPI4-2 channels. It is possible to support less than 24 ports in the following port counts: 16, 18, 20 or 22. To achieve these port counts the following port pairs must be enabled or disabled together: 0/16, 1/17, 2/18, 3/19, 4/20, 5/21, 6/22 or 7/23.

These ports must be enabled and disabled in pairs because the SPI4-2 Channels 0-7 are shared between the lower 8 MAC ports and the highest 8 MAC ports. When a channel is shared between two ports, for example Port 0 and Port 16 sharing Channel 0, the FIFO status of the two ports is logically combined and reported as one status to prevent overflow. When a port is disabled, the status is always reported as Satisfied. Thus the ports must be enabled and disabled in the specified pairs to prevent ports from being starved by the disabled port. For additional information on 16-Entry Calendar operation see “16-Entry Calendar Mode” in the Functional Description section of the Datasheet.

For additional product and ordering information:

www.cortina-systems.com

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