



# **Migration from the Cortina Systems® LXT9781 Transceiver to the Cortina Systems® LXT9785/9785E Transceiver**

**Application Note**

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**20 July 2007**

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## Revision History

<b>Revision 4.0</b> <b>Revision Date: 20 July 2006</b>
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<b>Revision 3.0</b> <b>Revision Date: 28 December 2006</b>
First release of this document from Cortina Systems, Inc.

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<ul style="list-style-type: none"><li>• Modified <a href="#">Section 1.0, Introduction</a>, on page 5 – changed PECL to LVPECL.</li><li>• Modified <a href="#">Table 1, Twisted-Pair/Fiber Interface Comparison</a>, on page 7.</li><li>• Replaced <a href="#">Figure 2, Network Fiber Interface Circuit Comparison</a>, on page 9.</li><li>• Removed <a href="#">Section 2.2, Signal Comparison of Twisted-Pair and Fiber Modes</a>.</li></ul>

<b>Revision 001</b> <b>Revision Date: 27 January 2005</b>
Initial release

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## 1.0 Introduction

LXT9785/9785E and LXT9781 8-port Fast Ethernet 10/100 Transceivers support IEEE 802.3 physical layer applications. Both devices provide a Reduced Media Independent Interface (RMII). In addition to the RMII feature, the LXT9785/9785E Transceiver is capable of providing both Serial and Source Synchronous Media Independent Interfaces (SMII/SS-SMII) for serial switching and other independent port applications.

While the LXT9785/9785E and LXT9781 Transceivers are similar in many respects, the LXT9785/9785E Transceiver incorporates several functional enhancements for a more robust Ethernet solution. This document provides an outline of the differences between the two devices and is intended to support design upgrades that take advantage of the LXT9785/9785E Transceiver to enhance existing LXT9781 Transceiver designs.

At the top level, the LXT9785/9785E and LXT9781 Transceivers provide substantially similar external interfaces:

- Both devices support twisted-pair operations via an internal twisted-pair PMD block.
- Both devices support fiber operations via a Low-Voltage Positive Emitter Coupled Logic (LVPECL) interface to external fiber modules that perform the PMD functions for fiber networks.
- Both devices use the same clock input.
- Both devices support JTAG.
- Both devices include a Bob Smith termination.

There are some significant differences between the two devices with respect to these external interfaces. These differences are listed in the following list of feature comparisons and discussed throughout the document.

### 1.1 Overview

#### 1.1.1 Feature Comparison

Comparisons of the feature sets of the LXT9785/9785E and LXT9781 Transceivers are grouped into the following three categories:

- Analog
- Digital
- General

#### 1.1.2 Analog Interface

- Receive and Transmit Load Termination
- Fiber
- RBIAS
- Magnetics and I/O
  - Magnetics for auto MDI/MDIX
  - Center tap voltage Levels

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### 1.1.3 Digital Interface

- CFG
- LEDs
  - Functional difference
  - Pin difference
- Serial LEDs
- Register Differences
- QSTAT
- RefClk
- MDC Frequency
- MII Sectionalization
- MII and RMII Interface Comparison
- Mode Select Requirements

### 1.1.4 General

- MAC Interfaces Supported
- Package Options
- Power Management
- Pin Assignment Comparison

## 2.0 Analog Interface

### 2.1 Twisted-Pair and Fiber Interfaces

The LXT9785/9785E and LXT9781 Transceivers have many of the same functionalities but there are some differences in twisted-pair and fiber interfaces. [Table 1](#) provides a comparison.

**Table 1 Twisted-Pair/Fiber Interface Comparison**

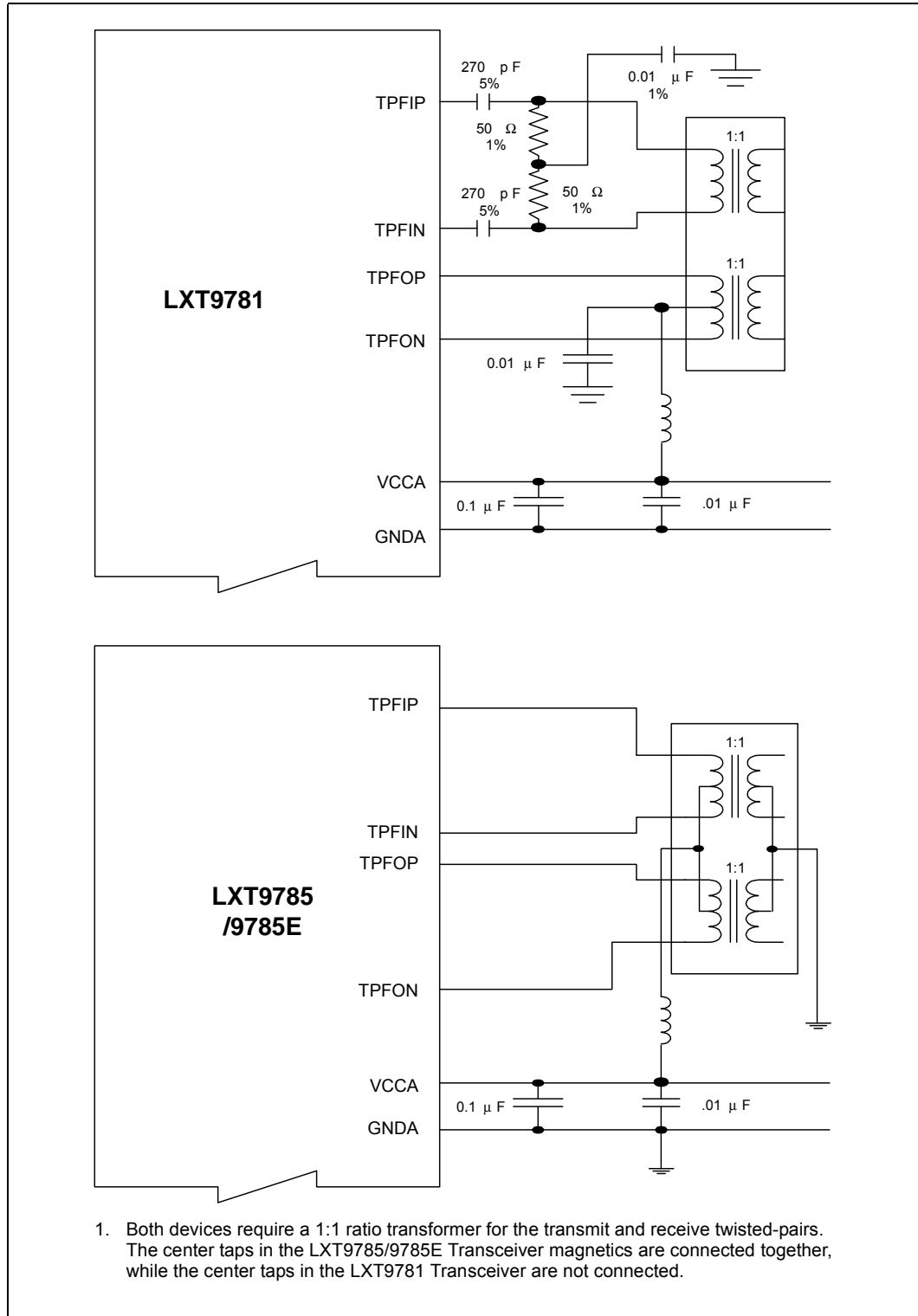
Function	LXT9781 Transceiver	LXT9785/9785E Transceiver
	Signal Description	Signal Description
Twisted-Pair Interface	Both devices support twisted-pair and fiber networks via a single set of pins. Pin assignments are the same. See <a href="#">Figure 1 on page 8</a> and <a href="#">Figure 2 on page 9</a> for external circuitry comparisons.	
Transmit Current Source	Both devices use current driver output stages. The driver current is provided from an external source.	
	Auto MDI/MDIX not supported.	Due to auto MDI/MDIX functionality of the LXT9785/9785E Transceiver, all magnetic center taps are connected.
Transmit and Receive Termination Circuitry	Requires external load-balancing resistors on the twisted-pair output.	The external load-balancing resistors are integrated in the LXT9785/9785E Transceiver.
Fiber Interface	Both devices support twisted-pair and fiber networks via a single set of pins. Pin assignments are the same. Fiber applications are supported via a Low-Voltage PECL (LVPECL) interface to external fiber modules.	
Media Configuration	All ports are selected for fiber or twisted-pair when configured via hardware (SD/TP), and can only be intermixed via software using Register bit 16.0.	All ports are selected for fiber or twisted-pair when configured via hardware (G_FX/TP), and can only be intermixed via software using Register bit 16.0.

[Table 2](#) provides a network line interface comparison for the LXT9785/9785E and LXT9781 Transceivers and [Figure 1 on page 8](#) and [Figure 2 on page 9](#) provide network interface circuit comparisons for the two devices.

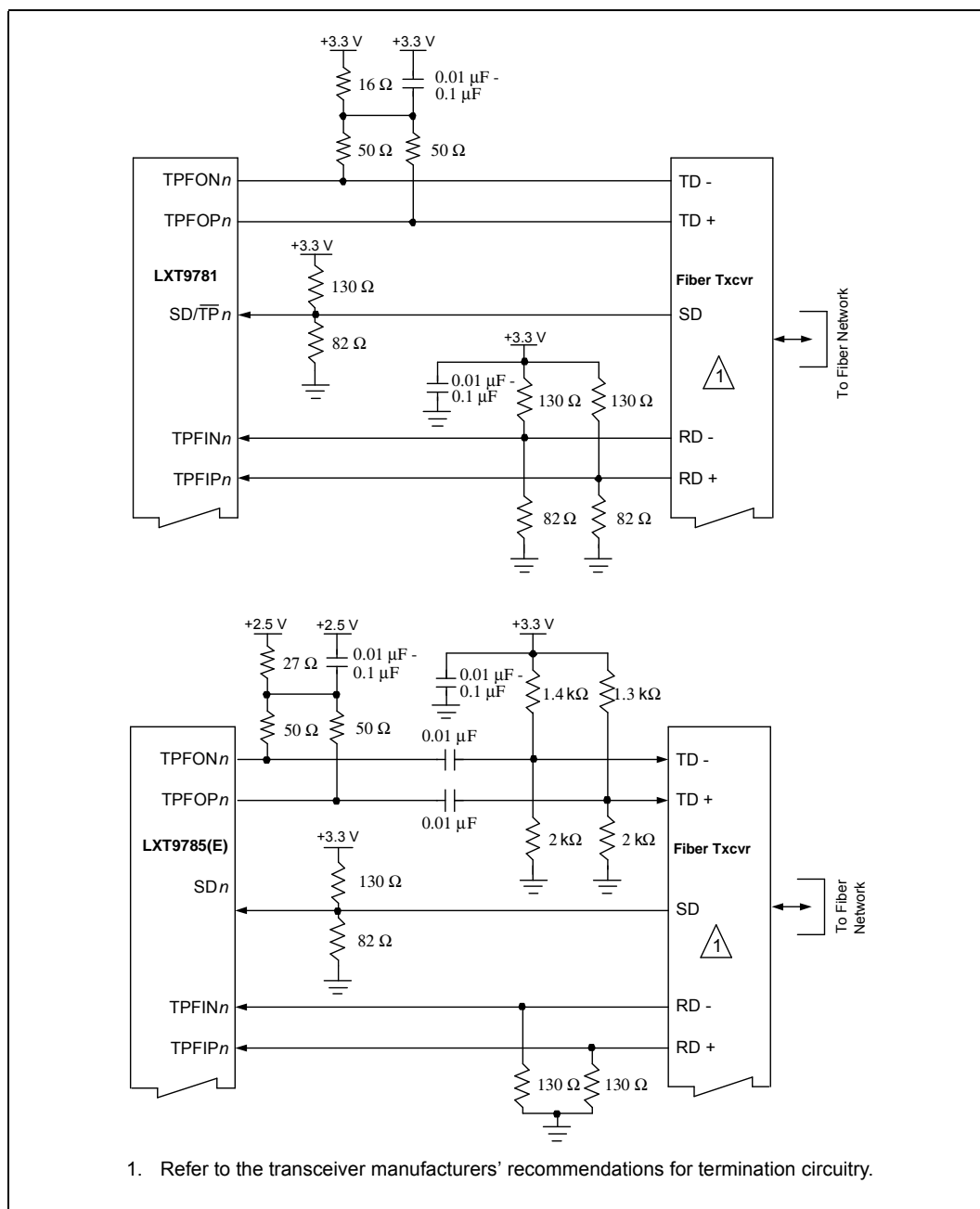
**Table 2 Network Line Interface Comparison**

Feature	LXT9781 Transceiver	LXT9785/9785E Transceiver
Auto MDI/MDIX	Not Supported	This feature automatically detects the link partner's transmitting cable pair, effectively allowing the connection of either a crossover cable or a patch cable to the device without additional external logic. May be disabled via Register bits 27.9:8, or by using the hardware configuration pins.

**Figure 1 Network Twisted-Pair Interface Circuit Comparison**



**Figure 2 Network Fiber Interface Circuit Comparison**



## 2.2 RBIAS

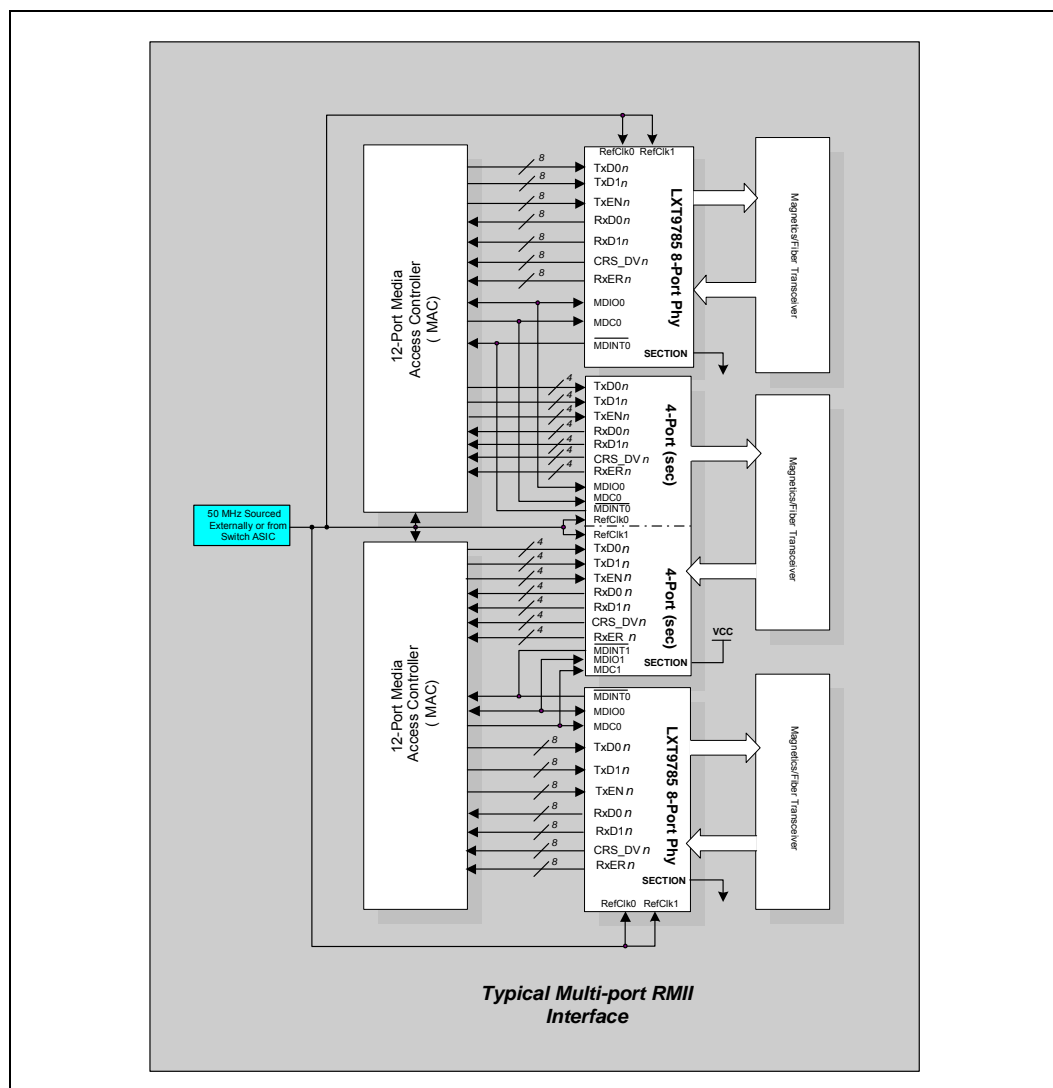
The RBIAS pin in the LXT9781 Transceiver provides bias current for internal circuitry that must be tied to ground through a 22.1KΩ 1% resistor. The RBIAS pin is integrated in the LXT9785/9785E Transceiver.

## 3.0 Digital Interface

### 3.1 Sectionalization

The LXT9785/9785E Transceiver supports a Sectionalization feature that is not supported by the LXT9781 Transceiver. This feature allows the chip to be sectionalized into two quad sections, splitting the MDIO bus into two separate PHY access ports. Ports 0-3 of the MDIO section operate independently of ports 4-7. The MII isolate function is unaffected and operates normally. Sectionalization is selected by pulling Section pin 176 High on the initial power-up sequence as seen in Figure 3. In applications needing sectionalization such as 1x8 or 2x4 that have a single MDIO bus structure, the addressing scheme must be contiguous. For example, the first eight ports are addressed with the base Address at 0 (0-7), so the next four ports must be addressed with the base Address at 8 (8-11).

**Figure 3 LXT9785/9785E Transceiver Typical RMI Multiport Interface**



### 3.2 Mode Controls and Indicators

Both the LXT9785/9785E and LXT9781 Transceivers support applications that use either Manual/Hardware control or MDIO/Software control. The design upgrade from the LXT9785/9785E and LXT9781 Transceivers is relatively simple. Table 3 provides a hardware/software control mode comparison.

**Table 3 Hardware/Software Control Mode Comparison**

Mode	Configuration	
	LXT9781 Transceiver	LXT9785/9785E Transceiver
<b>Manual/Hardware Control Mode</b> Both devices have identical settings. Refer to Table 4 for a comparison.		
MDDIS	For both devices, the operation of a physical interface consisting of a data line (MDIO) and clock line (MDC) is controlled by the MDDIS input pin. When MDDIS is Low, the MDIO port is enabled for both read and write operations.	
	When MDDIS is High, the MDIO is disabled from read and write operation.	When MDDIS is High, only the write operation is disabled on the MDIO bus.
<b>MDIO/Software Control Mode</b> Both devices support the IEEE 802.3 MDIO Management Interface.		
Clock Speed	Both devices require an external clock (MDC) to drive the MDIO interface.	
	Clock speed up to 8 MHz.	Clock speed has been increased up to 20 MHz to allow for faster control interface circuits.
RefClk	Both devices require a constant 50 MHz reference clock that must be enabled at all times.	

### 3.3 Hardware Configuration Settings

Table 4 provides a comparison of the hardware configuration settings for the LXT9785/9785E and LXT9781 Transceivers.

**Table 4 Hardware Configuration Settings (Sheet 1 of 2)**

Desired Mode			Required Settings					
			LXT9781 Transceiver Pin Settings LED/CFGn_1			LXT9785/9785E Transceiver Pin Settings CFG		
Auto-Neg	Speed	Duplex	1	2	3	CFG1	CFG2	CFG3
Disabled	10	Half	Low	Low	Low	Low	Low	Low
		Full	Low	Low	High	Low	Low	High
	100	Half	Low	High	Low	Low	High	Low
		Full	Low	High	High	Low	High	High

1. In the LXT9781 Transceiver, the Hardware Option uses three LED/CFG driver pins for each port while the LXT9785/9785E Transceiver uses one set of global pins per device. Refer to the Cortina Systems® LXT9785/9785E Transceiver datasheet and the Cortina Systems® LXT9781 Transceiver datasheet for detailed information.

**Table 4 Hardware Configuration Settings (Sheet 2 of 2)**

Desired Mode			Required Settings					
			LXT9781 Transceiver Pin Settings LED/CFGn_1			LXT9785/9785E Transceiver Pin Settings CFG		
Auto-Neg	Speed	Duplex	1	2	3	CFG1	CFG2	CFG3
Enabled	100 Only	Half	High	Low	Low	High	Low	Low
		Full	High	Low	High	High	Low	High
	10/100	Half Only	High	High	Low	High	High	Low
		Full or Half	High	High	High	High	High	High

1. In the LXT9781 Transceiver, the Hardware Option uses three LED/CFG driver pins for each port while the LXT9785/9785E Transceiver uses one set of global pins per device. Refer to the Cortina Systems® LXT9785/9785E Transceiver datasheet and the Cortina Systems® LXT9781 Transceiver datasheet for detailed information.

### 3.4 MII and Reduced MII (RMII) Interfaces

The Media Independent Interface (MII) and Reduced Media Independent Interface (RMII) for the LXT9785/9785E and LXT9781 Transceivers are compared in [Table 5](#).

**Table 5 MII and RMII Interface Comparison (Sheet 1 of 2)**

Feature	LXT9781 Transceiver	LXT9785/9785E Transceiver
<b>RMII Interface</b>		
RMII Data Interface	Both devices provide a separate RMII interface for each network port, complying with the RMII standard.	
Configuration Management Interface	Both devices provide an MDIO Management Interface.	
	Provides Hardware Control Interface via the LED/CFG pins.	Provides Hardware Control Interface via CFG pins (shown in <a href="#">Table 4</a> ).
<b>MII Interface</b>		
MII Addressing	Both devices support 5 pins for MII Addressing.	
MII Sectionalization	Not Supported.	Allows the device to be sectionalized into 1x8 or 2x4 (two quad sections). The MDIO bus splits into two separate PHY access ports (shown in <a href="#">Figure 3 on page 10</a> ).
MII Isolate	Not Supported.	In applications where the MII needs to be isolated from the bus, the RMII configuration is three-stated using Register bit 0.10 (refer to the LXT9785/9785E Transceiver datasheet).

**Table 5 MII and RMI Interface Comparison (Sheet 2 of 2)**

Feature	LXT9781 Transceiver	LXT9785/9785E Transceiver
MII Interrupts	Both devices provide two dedicated interrupt registers for each port. Register 18 of each PHY provides interrupt enable and Register 19 provides interrupt status. Setting bit 18.1=1 of each PHY enables a port to request interrupt via the MDINT pin. An active low on this pin indicates a status change on each PHY. Interrupts may be caused by any of the following conditions for each PHY:	
	LXT9781 Transceiver Interrupts	LXT9785/9785E Transceiver Interrupts
	<ul style="list-style-type: none"> <li>• Auto-Negotiation Complete</li> <li>• Speed Status Change</li> <li>• Duplex Status Change</li> <li>• Link Status Change</li> </ul>	<ul style="list-style-type: none"> <li>• Auto-Negotiation Complete</li> <li>• Speed Status Change</li> <li>• Duplex Status Change</li> <li>• Link Status Change</li> <li>• Isolate Status Change</li> </ul>
Link Establishment	Both devices support Auto-Negotiation, Base Page Exchange, Next Page Exchange, Link Criteria, and Parallel Detection.	

### 3.5 Register Set

Table 6 provides a comparison of Register Sets and Table 7 lists the register bits in the LXT9785/9785E and LXT9781 Transceivers for various common functionalities. Refer to the LXT9785/9785E Transceiver datasheet and LXT9781 Transceiver datasheet for comprehensive information on register sets.

**Table 6 LXT9785/9785E and LXT9781 Transceivers Register Set Comparison**

Register Address	LXT9781 Transceiver	LXT9785/9785E Transceiver (RMII Mode)
0 through 20	No Change	No Change
21	Reserved	Receive Error Count Register
22 - 26	No Change	No Change
27	Reserved	Trim Enable Register
28	Transmit Control Register #1	Reserved
29	No Change	No Change
30	Transmit Control Register #2	Reserved
31	No Change	No Change

**Table 7 LXT9785/9785E and LXT9781 Transceivers Register Bit Comparison**

Function	Name	Bit	Configuration	
			LXT9781 Transceiver	LXT9785/9785E Transceiver
Control	Isolate	0.10	Not available	1 = Electrically isolate PHY from RMII or SMII interface 0 = Normal Operation
Configuration	Bypass 4B5B (100BASE-TX)	16.11	Reserved	1 = Bypass 4B5B encoder and decoder 0 = Normal Operation
Quick Status	FIFO Error	17.6	Reserved	1 = FIFO error has occurred (overflow or underflow) 0 = No FIFO error has occurred
Interrupt	ISOLMSK	18.3	Reserved	Mask for Isolate Interrupt 1 = Enable event to cause interrupt 0 = Do not allow event to cause interrupt
	RxERCntFul	19.8	Reserved	RxER Counter Full Status 1 = One of the internal counters has reached its maximum value 0 = The internal counters have not reached maximum value.
	Isolate	19.3	Reserved	MII Isolate Change Status 1 = An isolate change has occurred since last reading this register 0 = An isolate change has not occurred since last reading this register.

### 3.6 LED Drivers

Both the LXT9785/9785E and LXT9781 Transceivers have three LED drivers. The function of each LED driver is selectable from the following list:

- Link
- Speed
- Transmit
- Receive
- Collision
- Duplex Status

The LED drivers can be programmed to display various combined status conditions. Refer to the LED Configuration Register tables in the Cortina Systems® LXT9785/9785E Transceiver datasheet and the Cortina Systems® LXT9781 Transceiver datasheet. [Table 8](#) compares the LED driver pins via their respective registers.

**Note:** Serial LEDs are supported for all ports in the LXT9781 Transceiver. The LXT9785/9785E Transceiver does not support this feature.

**Table 8 Comparison of LEDs**

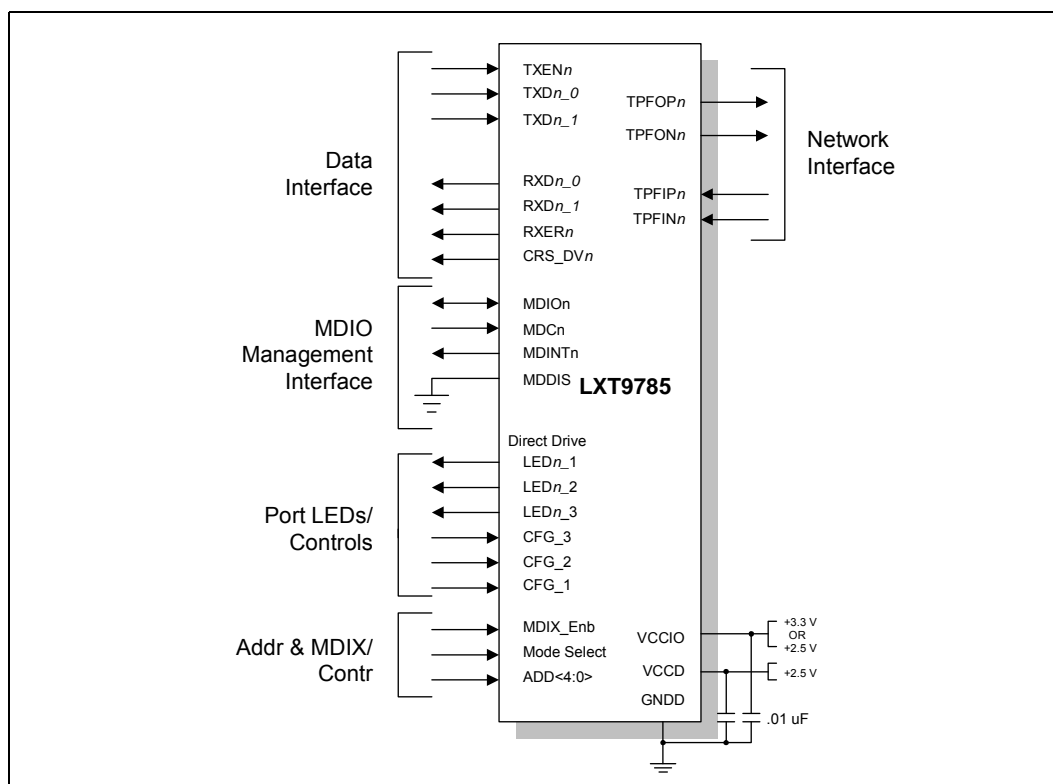
Register	Symbol	Configuration Status Bit	
		LXT9781 Transceiver	LXT9785/9785E Transceiver
20.15:12	LED1 Programming Bits	0110 = Reserved	0110 = Display Isolate Status
		1111 = Reserved	1111 = Display Link and Rx Error Status Combined
	Default	0000 = Display Speed Status	0000 = Display Speed Status
20.11:8	LED2 Programming Bits	0110 = Reserved	0110 = Display Isolate Status
		1111 = Reserved	1111 = Display Link and Rx Error Status Combined
	Default	0100 = Display Link Status	1101 = Display Link and Activity Status combined
20.7:4	LED3 Programming Bits	0110 = Reserved	0110 = Display Isolate Status
		1111 = Reserved	1111 = Display Link and Rx Error Status Combined
		0010 = Display Receive Status	1110 = Display Duplex and Collision Status combined
20.0	Reserved/INVPOL	INVPOL 1 = Use active High polarity for serial LEDs 2 = Use active Low polarity for serial LEDs	Reserved

## 4.0 General Interface

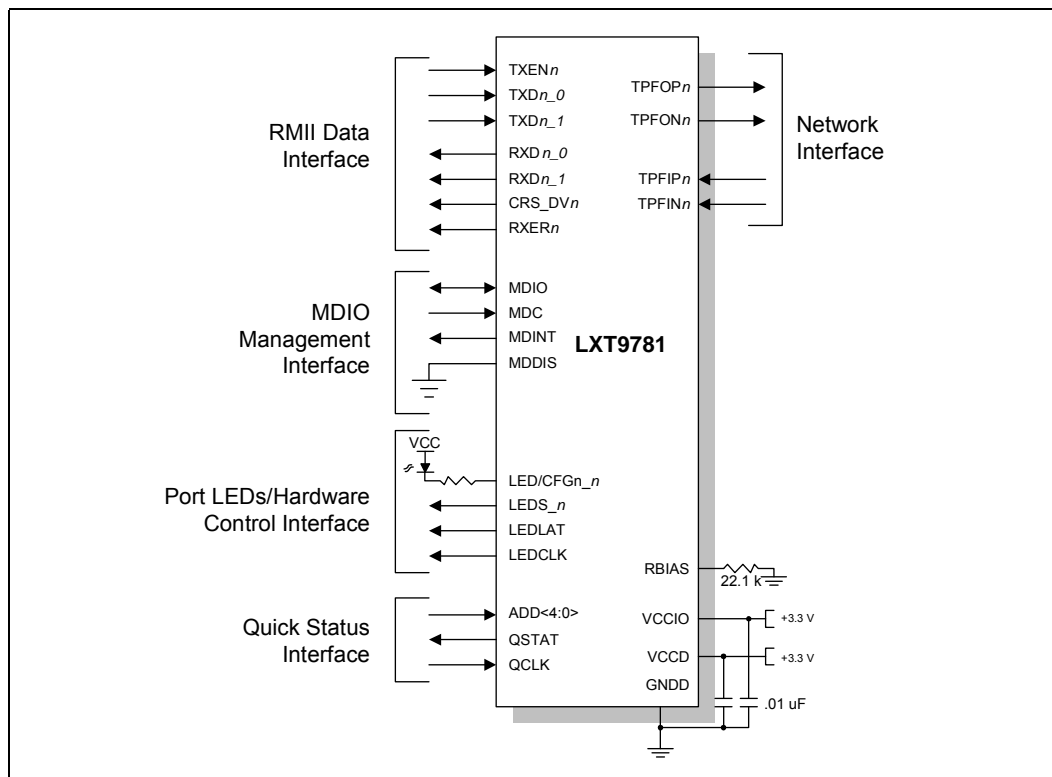
There is a high level of similarity between the LXT9785/9785E and LXT9781 Transceivers. The following bullets show some major differences between the two devices (see general interfaces in [Figure 4](#) and [Figure 5](#)).

- Since the RBIAS is terminated in the LXT9785/9785E Transceiver, there is no need for an external termination.
- The LXT9781 Transceiver requires three LEDs for each port while the LXT9785/9785E Transceiver only requires one LED/CFG pin for each port. As seen in [Figure 4](#), there is no external pull-up/pull-down requirement for the LED/CFG pins in the LXT9785/9785E Transceiver.
- The LXT9785/9785E Transceiver provides an auto MDI/MDIX feature that is not supported in the LXT9781 Transceiver.

**Figure 4 LXT9785/9785E Transceiver Interface**



**Figure 5 LXT9781 Transceiver Interface**



## 4.1 Power Management

Table 9 provides a comparison of power supplies, support for lower-voltage MACs, power-down mode, and transmit driver supply for both the LXT9785/9785E and LXT9781 Transceivers.

**Table 9 Power Management Comparison (Sheet 1 of 2)**

Function	Description	LXT9781 Transceiver	LXT9785/9785E Transceiver
<b>Power Supply</b>			
VCCIO	Digital Power Supply I/O Ring.	3.3 V	2.5 V/3.3 V
VCCD	Digital Power Supply Core.	3.3 V	2.5 V
VCCA	The common power supply for all analog circuits.	3.3 V (including all the transmit and receive circuits plus the magnetics center tap.)	2.5 V
GND	Common ground for all supplies.	Same	Same

**Table 9 Power Management Comparison (Sheet 2 of 2)**

Function	Description	LXT9781 Transceiver	LXT9785/9785E Transceiver
VCCPECL	Digital power supply - PECL Signal Detect Inputs.	Not supported.	+2.5 V/3.3 V supply for PECL signal detect input circuits. When fiber mode is not used, these pins are tied to GNDPECL to save power.
GNDPECL	Ground return for all PECL Signal Detect Input circuits.	Not supported.	Digital GND. PECL Signal Detect Input.
Support for Lower-Voltage MACs	Power supply input VCCIO supports the MII interface to the MAC controller.	Regardless of the I/O supply, digital I/O pins remain tolerant of 5 V signal levels.	Signals are tolerant to 3.3 V/ 5.0 V when the I/O supply is 3.3 V and 2.5 V/ 3.3 V/5.0 V when the I/O supply is 2.5 V.
Power-Down Mode	Both devices support a power-down mode that is enabled via an external input pin (the hardware global power-down) or per port via the MDIO Control Register. Power-down functionality is essentially the same for both devices.		
Transmit Driver Supply	Both devices use current-driven output states. This driver current can be supplied from an external 3.3 V or 2.5 V source. Using a 2.5 V source provides significant power savings.		

## 4.2 Production Support

The LXT9785/9785E and LXT9781 Transceivers have several features to enhance production including JTAG Boundary Scan and new packages for portable applications.

### 4.2.1 Boundary Scan

Both the LXT9785/9785E and LXT9781 Transceivers provide a JTAG 1149.1 boundary scan test port, providing direct access to every pin on the device and simplifying production test requirements. The standard requirement for 'bed of nails' test fixtures may be eliminated in many applications. This is particularly advantageous for applications using the BGA package.

### 4.2.2 Package and Temperature Options

Both the LXT9785/9785E and LXT9781 Transceivers are available in two packages, Plastic Quad Flat Pack (PQFP) and Plastic Ball-Grid Array (PBGA), and support a commercial operating temperature only.

### 4.2.3 Pin Assignments

Table 10 provides a pin-to-pin comparison to assist in design conversions.

**Table 10 LXT9785/9785E and LXT9781 Transceivers QFP Pin Assignment Comparison (Sheet 1 of 2)**

Pin #	Signal Name		Pin #	Signal Name		Pin #	Signal Name		Pin #	Signal Name	
	9781	9785		9781	9785		9781	9785		9781	9785
1	GNDD	CRS_DV6	53	GNDD	TXD1_1	105	TPFIN0	TPFIN0	157	TPFIP7	TPFIP7
2	RXD7_1	RXER6	54	RXD1_1	RXD0_1	106	VCCR	GNDRO	158	GND A	VCCR7
3	RXD7_0	TXEN6	55	RXD1_0	RXD0_0	107	TPFOP0	TPFOP0	159	SD/TP7	N/C
4	CRS_DV7	TXD6_0	56	CRS_DV1	VCCIO	108	TPFON0	TPFON0	160	SD/TP6	N/C
5	RXER7	TXD6_1	57	RXER1	GNDIO	109	GND A	VCCT0/1	161	SD/TP5	SD4
6	TXEN7	REFCLK1	58	TXEN1	CRS_DV0	110	TPFON1	TPFON1	162	SD/TP4	SD5
7	TXD7_0	RXD5_1	59	TXD1_0	RXER0/MDIX	111	TPFOP1	TPFOP1	163	TDI	GNDPECL
8	TXD7_1	RXD5_0	60	TXD1_1	TXEN0	112	VCCT	GNDR1	164	TDO	VCCPECL
9	RXD6_1	GNDIO	61	RXD0_1	TXD0_0	113	VCCR	GNDT0/1	165	TMS	SD6
10	RXD6_0	CRS_DV5	62	RXD0_0	TXD0_1	114	TPFIN1	TPFIN1	166	TCK	SD7
11	CRS_DV6	RXER5	63	CRS_DV0	MDC0	115	TPFIP1	TPFIP1	167	$\overline{\text{TRST}}$ TDI	
12	RXER6	TXEN5	64	RXER0	MDIO0	116	GND A	VCCR1	168	LEDCLK	TDO
13	TXEN6	TXD5_0	65	TXEN0	VCCD	117	GND A	VCCR2	169	LEDLATCH	TMS
14	TXD6_0	TXD5_1	66	TXD0_0	GNDD	118	TPFIP2	TPFIP2	170	LEDS7	TCK
15	VCCIO	RXD4_1	67	VCCIO	$\overline{\text{MDINT0}}$ 1	19	TPFIN2	TPFIN2	171	LEDS6	$\overline{\text{TRST}}$
16	GNDD	RXD4_0	68	GNDD	LED3_3	120	VCCR	GNDR2	172	LEDS5	N/C
17	TXD6_1	CRS_DV4	69	TXD0_1	LED3_2	121	TPFOP2	TPFOP2	173	LEDS4	$\overline{\text{G\_FX/TP}}$
18	TXD5_1	VCCIO	70	MDC	LED3_1	122	TPFON2	TPFON2	174	LEDS3	PWRDWN
19	RXD5_0	GNDIO	71	MDIO	LED2_3	123	GND A	VCCT2/3	175	LEDS2	$\overline{\text{RESET}}$
20	CRS_DV5	RXER4	72	GNDD	LED2_2	124	TPFON3	TPFON3	176	LEDS1	SECTION
21	RXER5	TXEN4	73	GNDD	LED2_1	125	TPFOP3	TPFOP3	177	LEDS0	MODESEL0
22	TXEN5	TXD4_0	74	GNDD	GNDIO	126	VCCT	GNDR3	178	GNDD	MODESEL1
23	TXD5_0	TXD4_1	75	GNDD	LED1_3	127	VCCR	GNDT2/3	179	VCCD	SGND
24	TXD5_1	MDC1	76	TxSLEW_0	LED1_2	128	TPFIN3	TPFIN3	180	LED/CFG7_1	LED4_1
25	RXD4_1	MDIO1	77	TxSLEW_1	LED1_1	129	TPFIP3	TPFIP3	181	LED/CFG7_2	LED4_2
26	RXD4_0	$\overline{\text{MDINT1}}$ 78		GNDS	VCCD	130	GND A	VCCR3	182	LED/CFG7_3	LED4_3
27	CRS_DV4	RXD3_1	79	PAUSE	GNDD	131	GND A	VCCR4	183	LED/CFG6_1	GNDD
28	RXER4	RXD3_0	80	VCCD	LED0_3	132	TPFIP4	TPFIP4	184	LED/CFG6_2	VCCD
29	TXEN4	VCCIO	81	GNDD	LED0_2	133	TPFIN4	TPFIN4	185	LED/CFG6_3	LED5_1
30	TXD4_0	GNDIO	82	PWRDWN	LED0_1	134	VCCR	GNDT4/5	186	LED/CFG5_1	LED5_2
31	VCCIO	CRS_DV3	83	$\overline{\text{RESET}}$ A	MDIX_EN	135	VCCT	GNDR4	187	LED/CFG5_2	LED5_3
32	GNDD	RXER3	84	MDINT	MDDIS	136	TPFOP4	TPFOP4	188	LED/CFG5_3	GNDIO
33	TXD4_1	TXEN3	85	MDDIS	CFG_3	137	TPFON4	TPFON4	189	LED/CFG4_1	LED6_1
34	RXD3_1	TXD3_0	86	GNDD	CFG_2	138	GND A	VCCT4/5	190	LED/CFG4_2	LED6_2
35	RXD3_0	TXD3_1	87	GNDD	CFG_1	139	TPFON5	TPFON5	191	LED/CFG4_3	LED6_3

**Table 10 LXT9785/9785E and LXT9781 Transceivers QFP Pin Assignment Comparison (Sheet 2 of 2)**

Pin #	Signal Name		Pin #	Signal Name		Pin #	Signal Name		Pin #	Signal Name	
	9781	9785		9781	9785		9781	9785		9781	9785
36	CRS_DV3	RXD2_1	88	VCCD	ADD_4	140	TPFOP5	TPFOP5	192	GNDD	LED7_1
37	RXER3	RXD2_0	89	GNDD	ADD_3	141	VCCR	GND5	193	VCCIO	LED7_2
38	TXEN3	GNDIO	90	GNDD	ADD_2	142	TPFIN5	TPFIN5	194	LED/CFG3_1	LED7_3
39	TXD3_0	CRS_DV2	91	GNDD	ADD_1	143	TPFIP5	TPFIP5	195	LED/CFG3_2	GNDD
40	TXD3_1	RXER2	92	REFCLK	ADD_0	144	GND4	VCCR5	196	LED/CFG3_3	VCCD
41	RXD2_1	TXEN2	93	ADD_0	TxSLEW_1	145	GND4	VCCR6	197	LED/CFG2_1	RXD7_1
42	RXD2_0	TXD2_0	94	ADD_1	TxSLEW_0	146	TPFIP6	TPFIP6	198	LED/CFG2_2	RXD7_0
43	CRS_DV2	TXD2_1	95	ADD_2	SD_2P5V	147	TPFIN6	TPFIN6	199	LED/CFG2_3	GNDIO
44	RXER2	REFCLK0	96	ADD_3	SD0	148	VCCR	GNDT6/7	200	LED/CFG1_1	CRS_DV7
45	TXEN2	RXD1_1	97	ADD_4	SD1	149	VCCT	GND6	201	LED/CFG1_2	RXER7
46	TXD2_0	RXD1_0	98	SD/TP3	VCCPECL	150	TPFOP6	TPFOP6	202	LED/CFG1_3	TXEN7
47	TXD2_1	VCCIO	99	SD/TP2	GNDPECL	151	TPFON6	TPFON6	203	LED/CFG0_1	TXD7_0
48	GNDD	GNDIO	100	SD/TP1	SD2	152	GND4	VCCT6/7	204	LED/CFG0_2	TXD7_1
49	GNDD	CRS_DV1	101	SD/TP0	SD3	153	TPFON7	TPFON7	205	LED/CFG0_3	RXD6_1
50	GNDD	RXER1/ PAUSE	102	RBIAS	N/C	154	TPFOP7	TPFOP7	206	QSTAT	RXD6_0
51	GNDD	TXEN1	103	GND4	VCCR0	155	VCCR	GND7	207	QCLK	GNDIO
52	VCCIO	TXD1_0	104	TPFIP0	TPFIP0	156	TPFIN7	TPFIN7	208	VCCIO	VCCIO



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