



Cortina Systems® LXT9785/LXT9785E PHY: Restart of Auto-Negotiation During Internal Loopback

Application Note

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Revision History

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Initial release.

1.0 Introduction

This Application Note is a detailed description of spurious packets received by the system interface after restarting auto-negotiation in internal loopback passing 100 Mbps data. Restarting auto-negotiation in internal loopback is not an intended mode of operation for the Cortina Systems® LXT9785 and LXT9785E 8-Port 10/100 Mbps PHY Transceiver (LXT9785/LXT9785E PHY).

The internal loopback function disables the twisted-pair (TP) drivers and prevents the LXT9785/LXT9785E PHY from generating fast link pulse (FLP) bursts, which are necessary to transmit and exchange auto-negotiation code words. The code words are required to complete an auto-negotiation process. The lack of code word exchange forces parallel detection to resolve the highest common link capability.

Internal loopback mode characteristics are described to understand the observations. Internal loopback is designed to disable the analog TP driver and receiver to isolate the LXT9785/LXT9785E PHY from the cable connection and any link partner. This prevents data from being transmitted onto or received from the network. The digital 10/100 Mbps transmit circuits are internally looped back to the respective digital receive circuits. Auto-negotiation enables the 10BASE-T receive path and allows the 100BASE-T transmit data to be output as 10BASE-T data on the switch interface until auto-negotiation completes and a 100 Mbps link is established. Unauthentic data is output until the 100 Mbps link is established. Valid 100 Mbps data is sent out on the SMI interface to the switch engine after link establishment.

2.0 Detailed Description

This section describes in detail what happens when the 100 Mbps internal loopback is enabled and auto-negotiation is restarted while 100 Mbps data is transmitted to the LXT9785/LXT9785E PHY. The operation is explained in the following order:

1. 100 Mbps internal loopback operation ([Section 2.1, page 5](#))
2. Auto-negotiation is restarted ([Section 2.2, page 6](#))
3. 100 Mbps data is looped back as 10 Mbps data ([Section 2.3, page 6](#))
4. Parallel detection completes and 100 Mbps link is established ([Section 2.4, page 7](#))
5. Limitations ([Section 2.5, page 8](#))

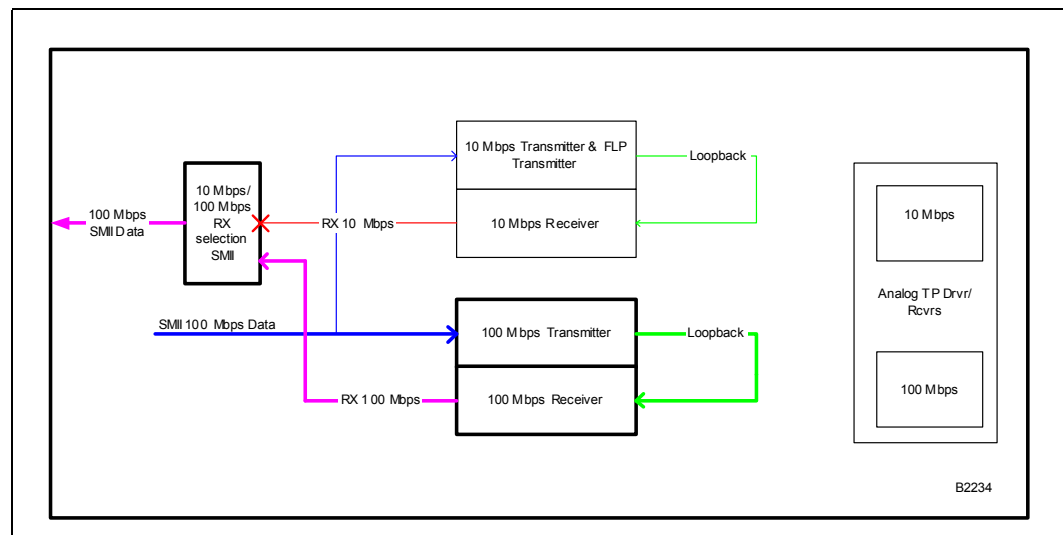
2.1 100 Mbps Internal Loopback Operation

When internal loopback is enabled, all data transmitted at the switch engine through the SMI interface is allowed to loop back through the digital 10 Mbps and 100 Mbps transmit and receive paths. The data does not pass through the TP analog driver.

[Figure 1](#) shows a simple diagram of the 100 Mbps internal loopback path. The 100 Mbps data from the switch interface is sent in through the 100 Mbps transmitter and looped back through the 100 Mbps receiver. The data is sent to 10/100 Mbps RX selection logic, which selects the 100 Mbps data since the device is in 100 Mbps loopback mode.

Note: No data is driven onto the network in internal loopback mode.

Figure 1 Standard 100 Mbps Internal Loopback Operation

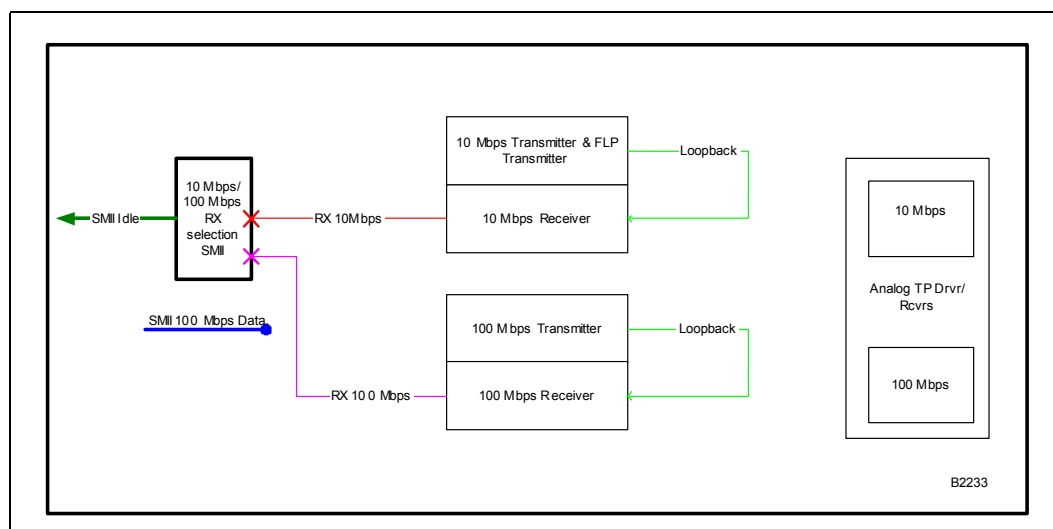


2.2 Restarting Auto-Negotiation

When auto-negotiation is restarted, the Break Link Timer (BLT) is started and the LXT9785/LXT9785E PHY is forced to 10 Mbps operation as required to enable the auto-negotiation process. The SMII receive data interface is forced to the idle state. All incoming data from the switch engine on the SMII transmit path is ignored. After the BLT timer expires (1.2 s - 1.5 s), the auto-negotiation algorithm enables the 10 Mbps SMII receive interface and the parallel detection algorithms for both the 10 Mbps and 100 Mbps receivers. These events are required to implement the auto-negotiation standard.

Figure 2 shows what happens when auto-negotiation is restarted during internal loopback. Until the BLT expires, all data coming in on the SMII transmit path is ignored and the receive SMII is forced to the idle state.

Figure 2 100 Mbps Internal Loopback Auto-Negotiation Restarted and Link Break Timer Is Active

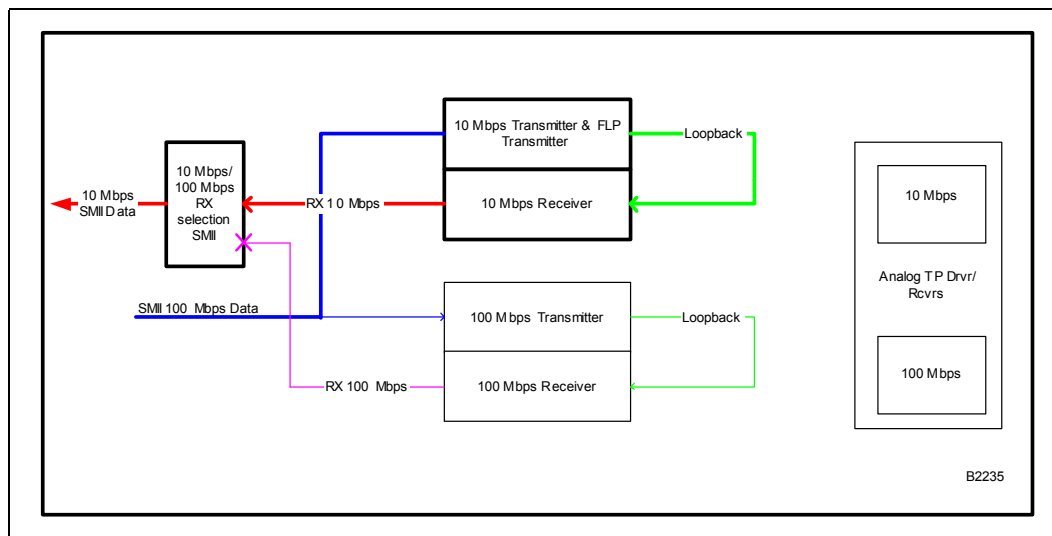


2.3 100 Mbps Data Looped Back As 10 Mbps Data

Until parallel detection is completed, the 100 Mbps data driven on the SMII interface by the switch engine is sampled at 10 Mbps and is transmitted as a packet by the 10 Mbps transmit logic. The 10 Mbps packet contains only a portion of the original valid 100 Mbps data. Its length will be decimated (reduced by a factor of 10) because in 10 Mbps mode, the data input to the LXT9785/LXT9785E PHY is only sampled once every ten sync pulse frames per the 10 Mbps portion of the SMII specification. The packet will not contain valid data. The internal loopback function loops the packets back to the 10 Mbps receiver. Since the SMII receive interface is enabled for 10 Mbps operation, the spurious packet data is output on the switch interface as 10 Mbps packets. The SMII receive data may consist of fragments, alignment errors, CRC errors, or any similar type of error. The corrupted data is looped back, is not sent out onto the network, and is only seen on the receive SMII interface.

Figure 3 shows how the 100 Mbps data is looped back as 10 Mbps data. Since the LXT9785/LXT9785E PHY is in 10 Mbps during auto-negotiation, the 10/100 Mbps RX selection logic sends the 10 Mbps data to the SMII interface.

Figure 3 100 Mbps Loopback, 100 Mbps Data Looped Back As 10 Mbps Data

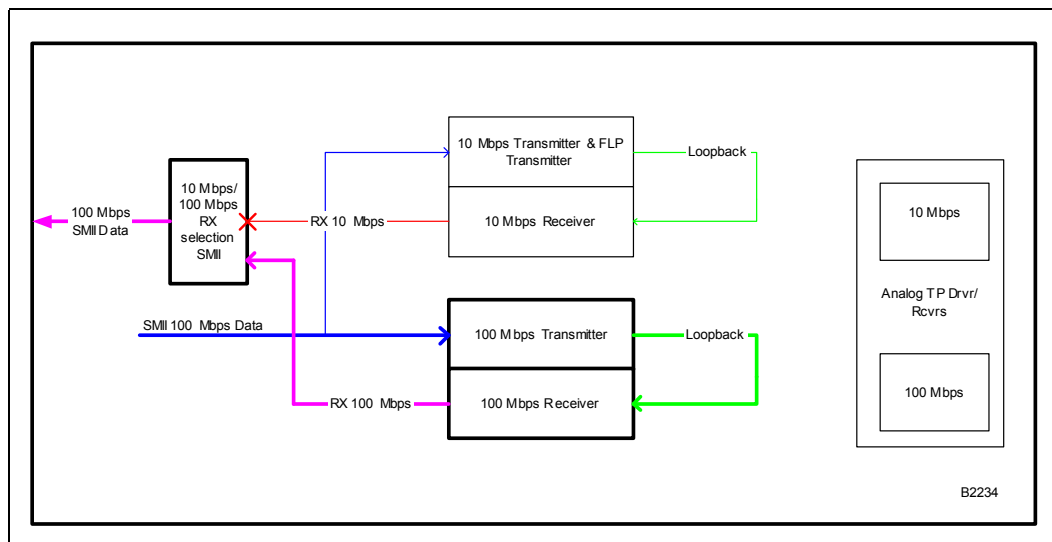


2.4 Parallel Detection Completed, 100 Mbps Link Established

The 100 Mbps packet data being driven on the SMII interface by the switch engine is also simultaneously input to the 100 Mbps transmit logic. The auto-negotiation process and the internal loopback function prevent the transmit logic from driving packets onto the network. The 100 Mbps receive output to the SMII interface is disabled and cannot be enabled until 100 Mbps parallel detection completes. 100 Mbps idles may create a temporary 10 Mbps link, but internal logic prevents a permanent 10 Mbps link from occurring from 100 Mbps idles. The 100 Mbps packets looped back to the receiver cause the parallel detection state to be entered for 100 Mbps. A 100 Mbps link is typically brought up, the 10 Mbps data path is disabled, the 100 Mbps data path is enabled, and valid 100 Mbps packets are output on the SMII receive interface. Internal loopback operates without errors from this point forward.

Figure 4 shows a diagram of the 100 Mbps loopback path after parallel detection completes. This diagram shows the 100 Mbps data from the SMII is sent in through the 100 Mbps Transmitter and looped back through the 100 Mbps receiver. The data is then sent to 10/100 Mbps RX selection logic, which selects the 100 Mbps data since the device is now operating normally in 100 Mbps loopback mode.

Figure 4 100 Mbps Loopback Operates Normally After Parallel Detection Complete



2.5 Limitations

There are some limitations that determine if link is brought up. Parallel detection requires half-duplex be advertised at the detected speed for link establishment. If Register 4 (Auto-Negotiation Advertisement) advertises half-duplex for the speed detected, 100 Mbps link is brought up and the valid 100 Mbps data is driven onto the receive SMII interface. If Register 4 is programmed only to advertise full-duplex for the detected speed, link will not establish. Link does not establish under these conditions because parallel detection requires the resulting link to operate in half-duplex. The link is not advertising this capability and there is no Highest Common Denominator (required by the auto-negotiation standard for link establishment).

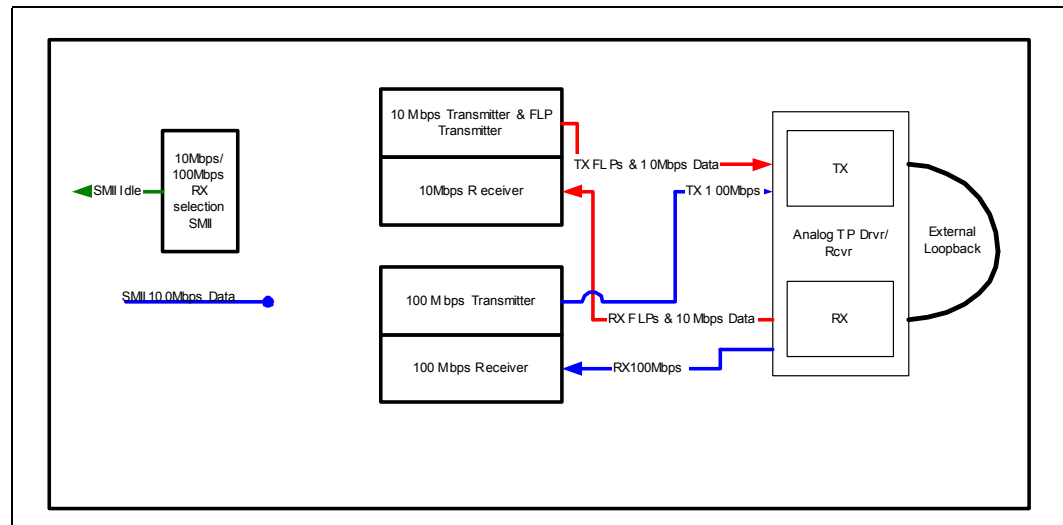
If a 100 Mbps link is not established, the LXT9785/LXT9785E PHY remains in 10 Mbps mode and all 100 Mbps input to the SMII transmit path will create errors when looped back.

3.0 External Loopback

The 10 Mbps invalid packets on the SMII receive interface do not occur in an external loopback cable application. The receive data path remains disabled at the 10 Mbps and 100 Mbps receiver until the completion of auto-negotiation code word exchange or 10 Mbps or 100 Mbps parallel detection. After the completion of this state, link comes up and allows data to be output on the SMII receive interface. When internal loopback is not enabled (as in an external loopback application), the 10 Mbps receiver does not receive packets directly from the transmit logic and data is passed back to the switch engine through the SMII interface.

Figure 5 shows external loopback during auto-negotiation and parallel detection. Until a 100 Mbps link is established, the 100 Mbps data input from the SMII interface is not transmitted out and nothing is sent out of the 10 Mbps or 100 Mbps receivers until a valid link is established.

Figure 5 External Loopback During Auto Negotiation/Parallel Detection





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