



# Cortina Systems<sup>®</sup> IXF1104 Quad-Port Gigabit Ethernet Media Access Controller

Design and Layout Guide: CBGA

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## Revision History

<b>Revision 7.0</b> <b>Revision Date: 30 April 2007</b>
First release of this document from Cortina Systems, Inc.

<b>Revision 006</b> <b>Revision Date: 19 July 2005</b>
<ul style="list-style-type: none"><li>• Added new <a href="#">Section 1.1, References, on page 6</a>.</li><li>• Removed old Section 2.7, "Clock Requirements" [old section 2.7.1 now becomes <a href="#">Section 2.7, Clock Layout Guidelines, on page 11</a>].</li><li>• Removed/modified text under <a href="#">Section 2.9, Open Drain I/O, on page 13</a>.</li><li>• Changed Table note 1 into Table notes 1 and 2 in <a href="#">Table 5, Recommended JTAG Termination, on page 14</a>.</li><li>• Modified text under <a href="#">Section 4.1, SPI3, on page 18</a>.</li><li>• Added the RENB_3:0 signal to the receive signals column in <a href="#">Table 6, Data Path Signals, on page 18</a>.</li><li>• Changed "path" to "signal" under <a href="#">Section 4.1.2, FIFO Status Signals, on page 19</a>.</li><li>• Removed Receive column and edited title in <a href="#">Table 7, SPI3 FIFO Status Signals, on page 19</a>.</li><li>• Added bullet under <a href="#">Section 4.1.3, SPI3 PCB Routing, on page 19</a> In a transmission trace, include a 50 <math>\Omega</math> series termination close to the source output drivers."</li></ul>

<b>Revision 005</b> <b>Revision Date: 17 February 2004</b>
<ul style="list-style-type: none"><li>• Modified first paragraph under <a href="#">Section 1.0, "General Description"</a>: [Broke into bullets and added OMI text].</li><li>• Added last bullet under <a href="#">Section 2.7.1, "Clock Layout Guidelines"</a></li><li>• Modified <a href="#">Figure 2 "Power Supply Filter Network"</a>: [Changed references from SerDes and PLL power balls to Analog power balls.]</li><li>• Added <a href="#">Table 1 "Analog Power Balls"</a>.</li><li>• Added new section: <a href="#">Section 2.8, "GMII, RGMII, and SerDes/OMI Multiplexed Ball Connections"</a>.</li><li>• Added new section: <a href="#">Section 2.9, "Open Drain I/O"</a>.</li><li>• Added new section: <a href="#">Section 2.10, "Boundary Scan (JTAG) Interface"</a>.</li><li>• Modified <a href="#">Section 3.3, "Power Supply Sequencing"</a>: Clarified power-up and power down sequence.</li><li>• Modified <a href="#">Table 7 "SPI3 PCB Trace Specifications"</a>: Removed Differential Trace Separation and Trace Length.</li><li>• Modified <a href="#">Section 4.2, "RGMII"</a>: Changed 2.5 V CMOS to 2.5 V CMOS (3.3 V compatible).</li><li>• Modified <a href="#">Section 4.3, "GMII"</a>: Updated the introduction.</li><li>• Modified <a href="#">Section 4.4, "SerDes"</a>: Added more information regarding the AC/DC coupling register, updated the routing constraints, and updated the SerDES PCB trace spec table.</li><li>• Added <a href="#">Figure 6 "552-Ball CBGA Ballmap"</a></li></ul>

<b>Revision 004</b> <b>Revision Date: 20 February 2003</b>
Added cautionary note to <a href="#">Section 5.0, "Device Package Footprint"</a>

<b>Revision 003</b> <b>Revision Date: 06 February 2003</b>
Changed <a href="#">Figure 5 "552-Ball CBGA PCB Pad Design"</a> including dimensions.



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<b>Revision 002</b> <b>Revision Date: 31 January 2002</b>
Edited 1.8 V and 2.5 V power up sequence in <a href="#">Section 3.3, "Power Supply Sequencing"</a>
<b>Revision 001</b> <b>Revision Date: 19 December 2002</b>
Initial release.

## 1.0 General Description

The Cortina Systems® IXF1104 Quad-Port Gigabit Ethernet Media Access Controller (IXF1104 MAC) supports the IEEE 802.3 10 Mbps, 100 Mbps, and 1000 Mbps applications. The IXF1104 MAC supports the following interfaces:

- System Packet Interface Level 3 (SPI3) interface with support for single-PHY (SPHY) and multi-PHY (MPHY) network processor connections
- Reduced Gigabit Media Independent Interface (RGMI [10/100/1000 Mbps])
- Gigabit Media Independent Interface (GMII [1000 Mbps])
- Serializer/Deserializer (SerDes [1000 Mbps]) for the physical media interface with an Optical Module Interface (OMI) for direct connection to optical modules

This application note provides design and layout guidelines to achieve optimum performance in high-density systems using the IXF1104 MAC. Adhering to these guidelines helps to ensure a successful design.

The following IXF1104 MAC topics are discussed in this document:

- [Section 2.0, General Design Guidelines](#): Outlines good design practices. Good design practices prevent most common signal and noise issues. Follow the general guidelines listed in this section throughout the entire design.
- [Section 3.0, Power and Ground Design](#): Focuses on power and ground plane layouts and internal routing of power and ground signals.
- [Section 4.0, Interfaces](#): Comprises the following four subsections:
  - [Section 4.1, SPI3](#): Describes the routing of the SPI3 interface between the IXF1104 MAC and the Network Processor/Forwarding Engine
  - [Section 4.2, RGMI](#): Describes the RGMI interface
  - [Section 4.3, GMII](#): Describes the GMII interface
  - [Section 4.4, SerDes](#): Describes the SerDes interface
- [Section 5.0, Device Package Footprint](#): Contains packaging and ball map diagrams.

## 1.1 References

Refer to [Table 1](#) for additional IXF1104 MAC information.

**Table 1 Documents and Relevant Links**

Documents and Relevant Links	Document Number
Cortina Systems® IXF1104 Quad Port Gigabit Ethernet Media Access Controller Datasheet	278757
Cortina Systems® IXF1104 Quad Port Gigabit Ethernet Media Access Controller Specification Update	278756
Cortina Systems® IXF1104 Media Access Controller SPI3 Performance Application Note	280046

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## 2.0 General Design Guidelines

### 2.1 Introduction

Meeting system performance requirements depends on good design practices. Good design practices minimize high-speed digital-switching and common-mode noise, and provide shielding between internal circuits and the environment.

To achieve maximum results, apply good design practices throughout the entire design process, not just to the IXF1104 MAC. [Section 2.2](#) through [Section 2.7, Clock Layout Guidelines, on page 11](#) outline recommended design practices.

### 2.2 General Recommendations

#### 2.2.1 Printed Circuit Board

High-speed SPI3, SerDes, and RGMII/GMII interfaces require a multi-layer Printed Circuit Board (PCB). Careful attention to trace layouts provides adequate signal integrity, including trace lengths, impedances, and terminations. In addition, the 552-ball Ceramic Ball Grid Array (CBGA) package requires multiple PCB trace layers to accommodate routing of all signals.

A typical PCB stack-up designed for the IXF1104 MAC requires 8 to 12 layers (see [Figure 1](#)).

**Figure 1 PCB Layout**

<u>LAYER STRUCTURE</u>		
Scale: None		
<u>Thickness in mils</u>		<u>Layer Number/Type</u>
0.33	0.25 oz.	Layer 1 -- Component
3	PRE-PREG	
1.2	0.5 oz.	Layer 2 -- Ground 1
3	CORE	
0.6	0.5 oz.	Layer 3 -- Signal 1
5	PRE-PREG	
1.2	0.5 oz.	Layer 4 -- Power 1
3	CORE	
0.6	0.5 oz.	Layer 5 -- Signal 2
5	PRE-PREG	
1.2	0.5 oz.	Layer 6 -- Power 2
39	CORE	
1.2	0.5 oz.	Layer 7 -- Ground 2
5	PRE-PREG	
0.6	0.5 oz.	Layer 8 -- Signal 3
3	CORE	
1.2	0.5 oz.	Layer 9 -- Ground 3
5	PRE-PREG	
0.6	0.5 oz.	Layer 10 -- Signal 4
3	CORE	
1.2	0.5 oz.	Layer 11 -- Power 3
3	PRE-PREG	
0.33	0.25 oz.	Layer 12 -- Solder

### 2.2.2 Components

Components must be verified to meet the entire application requirement. Use the information contained in the Cortina Systems® IXF1104 Quad-Port Gigabit Ethernet Media Access Controller (IXF1104 MAC) Datasheet as a reference only.

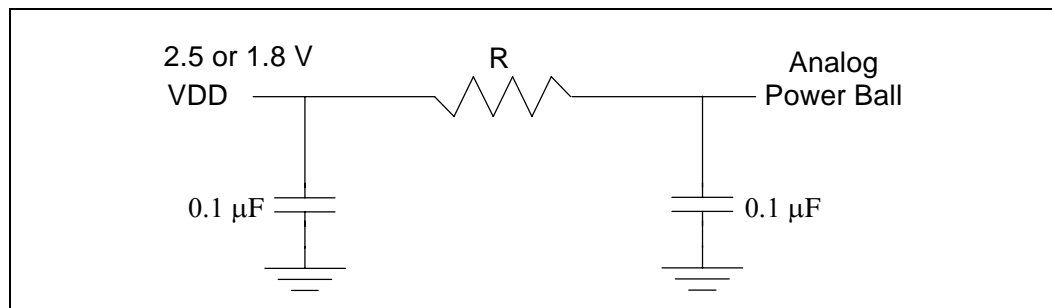
## 2.3 Power and Ground Filtering

The following are design and layout recommendations for power and ground filtering:

- Follow good design practices to minimize noise from digital-switching and power-supply circuits.
- Ensure the power supply is rated for the load.
- Keep power and ground noise levels below 50 mV.
- Filter and shield DC-DC converters and oscillators.
- Filter the analog power circuits.
  - Each analog power pin must have separate filter networks placed as close as possible to the respective power ball.

Refer to [Figure 2](#) and [Table 2](#) for the power supply filter network and analog power balls.

**Figure 2** Power Supply Filter Network



**Table 2** Analog Power Balls

Signal Name	Ball Designator	Comments
AVDD1P8_1	A5, A20	A filter must be provided (see <a href="#">Figure 2</a> ).
AVDD2P5_1	AD20	R: AVDD1P8_1 and AVDD2P5_1 = 5.6 Ω resistor.
AVDD1P8_2	AB16, T23	A filter must be provided (see <a href="#">Figure 2</a> ).
AVDD2P5_2	U14, R18	R: AVDD1P8_2 and AVDD2P5_2 = 1.0 Ω resistor.

## 2.4 Decoupling and Bulk Caps

The following are design and layout recommendations for decoupling and bulk caps:

- To minimize power-supply switching noise, use bulk capacitors (4.7-10 μF) between the power and ground planes.
- Use an ample supply of .01 μF decoupling capacitors to reduce high-frequency noise on the power and ground planes.
- To minimize or eliminate stubs, place decoupling capacitors between the signal ball and the corresponding reference ball (power/ground), and as close to the device as possible.

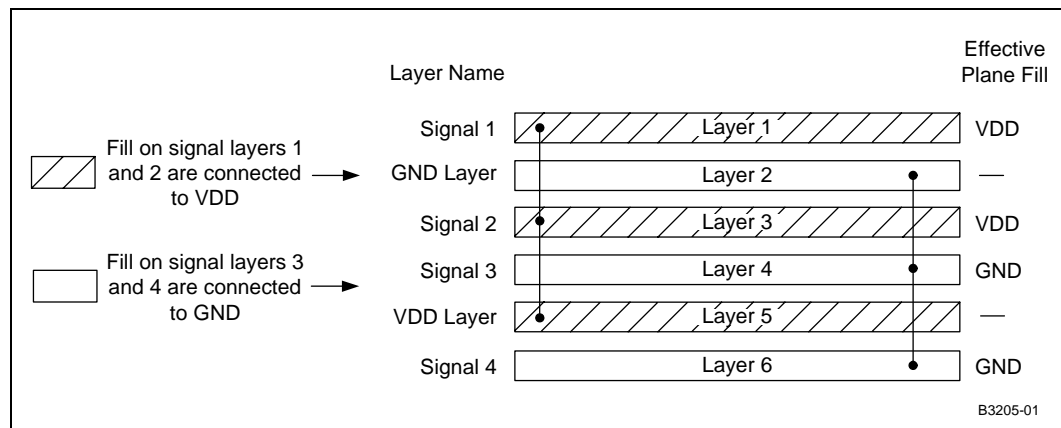
## 2.5 Power and Ground Planes

The following are design and layout recommendations for power and ground planes:

- Provide solid power and ground planes. Cuts in slots or planes degrade performance.
- Avoid breaks in the ground plane, especially in areas where the plane shields high-frequency signals.
- Route high-speed signals adjacent to a continuous, unbroken ground plane.
- Stagger vias to avoid creating moats caused by anti-pad voids in the planes.
- Whenever possible, fill in unused areas of the signal planes with solid copper. Attach them with vias to a VDD or ground plane that is not adjacent to the signal layer. This technique is called signal layer filling and can improve power plane capacitive coupling.

Figure 3 illustrates the signal layer fill.

**Figure 3** Signal Layer Fill



## 2.6 Differential Signal Layout

The following are design and layout recommendations for differential signal layout:

- Route differential pairs close together, equidistant and away from other signals.
- Keep each differential pair on the same plane.
- Minimize vias and layer changes.
- Keep transmit and receive pairs away from each other by running them orthogonally, or separating them with a ground plane layer.

## 2.7 Clock Layout Guidelines

The following are design and layout recommendations for the clock layout:

- Keep the clock traces as short as possible.
- Route the clock traces adjacent to an unbroken ground plane.
- Use a multi-output clock driver or buffer when driving multiple inputs with a single oscillator.
- Individually terminate point-to-point interconnections to every clock load. Series termination is the most common termination technique. Place the termination resistor as close to the driving source as possible.
- Route the clock traces as 50  $\Omega$  strip-line traces to minimize EMI.
- Minimize vias and layer changes.

## 2.8 GMII, RGMII, and SerDes/OMI Multiplexed Ball Connections

Table 3 lists the balls used for the line-side interfaces (GMII, RGMII, SerDes/OMI). Some balls are multiplexed and the operation depends on the mode selected for each port. Table 3 also provides a guide on connecting these balls.

**Note:** Do not connect any balls marked as no connect (NC).

**Table 3 Line Side Interface Multiplexed Balls (Sheet 1 of 2)**

Copper Mode		Fiber Mode	Unused Port	Ball Designator			
GMII Signal	RGMII Signal	Optical Module/ SerDes Signal					
TXC_3:0	TXC_3:0	NC	NC	AB14	AC20	AD7	AA1
TXD[3:0]_3 TXD[3:0]_2 TXD[3:0]_1 TXD[3:0]_0	TD[3:0]_3 TD[3:0]_2 TD[3:0]_1 TD[3:0]_0	NC	NC	V17 AB23 AD9 AA3	V16 AB22 AB9 Y3	V15 AB21 AB7 Y2	V14 AB20 AC7 Y1
TXD4_3:0	NC	TX_DISABLE_3:0 <sup>2</sup>	NC	AA14	AD16	AA7	AB3
TXD[7:5]_3 TXD[7:5]_2 TXD[7:5]_1 TXD[7:5]_0	NC	NC	NC	W14 AA18 AC9 Y4	AA16 AA20 AD8 AB4	Y15 AB19 AB8 AC3	– – – –
TX_EN_3:0	TX_CTL_3:0	NC	NC	V12	AC22	Y8	AB2
TX_ER_3:0	NC	NC	NC	AB13	AD17	AD6	W1
RXC_3:0	RXC_3:0	GND	GND	V23	AA24	AD11	V4
RXD[3:0]_3 RXD[3:0]_2 RXD[3:0]_1 RXD[3:0]_0	RD[3:0]_3 RD[3:0]_2 RD[3:0]_1 RD[3:0]_0	GND	GND	W18 Y23 W9 Y7	Y19 Y22 W11 W7	Y18 Y21 Y11 V7	Y17 Y20 Y9 V8
<p>1. An external pull-up resistor is required with most optical modules.                  2. An open drain I/O, external 4.7 k<math>\Omega</math> pull-up resistor is required.  <b>Note:</b> Refer to the Cortina Systems<sup>®</sup> IXF1104 Quad-Port Gigabit Ethernet Media Access Controller (IXF1104 MAC) Datasheet for a complete ball list.</p>							

**Table 3 Line Side Interface Multiplexed Balls (Sheet 2 of 2)**

Copper Mode		Fiber Mode	Unused Port	Ball Designator			
GMII Signal	RGMII Signal	Optical Module/ SerDes Signal					
RXD4_3:0	GND	MOD_DEF_3:0 <sup>1</sup>	GND	T16	W22	AD10	Y6
RXD5_3:0	GND	TX_FAULT_3:0 <sup>1</sup>	GND	T17	V20	AC11	Y5
RXD6_3:0	GND	RX_LOS_3:0 <sup>1</sup>	GND	T18	V19	AA11	AB5
RXD7_3:0	GND	GND	GND	T19	W20	Y10	AC5
RX_DV_3:0	RX_CTL_3:0	GND	GND	V18	Y24	AB11	V5
RX_ER_3:0	GND	GND	GND	U20	AA22	Y12	W5
CRS_3:0	GND	GND	GND	AC16	AB15	AA9	AA5
COL_3:0	GND	GND	GND	AB17	AD15	AB10	AB6
GND	GND	RX_P_3:0	GND	U24	T24	V22	P22
GND	GND	RX_N_3:0	GND	V24	R24	U22	R22
NC	NC	TX_P_3:0	NC	AC18	W16	AD13	Y13
NC	NC	TX_N_3:0	NC	AD18	Y16	AD14	Y14
NC	NC	TX_FAULT_INT <sup>2</sup>	NC	P23	–	–	–
NC	NC	RX_LOS_INT <sup>2</sup>	NC	P19	–	–	–
NC	NC	MOD_DEF_INT <sup>2</sup>	NC	N22	–	–	–
MDC	MDC	NC	NC	W24	–	–	–
MDIO	MDIO <sup>2</sup>	NC	NC	V21	–	–	–
NC	NC	I <sup>2</sup> C_CLK	NC	L23	–	–	–
NC	NC	I <sup>2</sup> C_DATA_3:0 <sup>2</sup>	NC	P24	N24	M24	L24

1. An external pull-up resistor is required with most optical modules.  
2. An open drain I/O, external 4.7 kΩ pull-up resistor is required.  
**Note:** Refer to the Cortina Systems® IXF1104 Quad-Port Gigabit Ethernet Media Access Controller (IXF1104 MAC) Datasheet for a complete ball list.

## 2.9 Open Drain I/O

Table 4 lists the open drain Inputs/Outputs (I/Os). All IXF1104 MAC open drain I/Os designated in Table 4 can operate as open drain I/Os or as a push/pull drivers. In normal operation, these I/Os operate as open drain.

Cortina recommends that all IXF1104 MAC open drain I/Os use separate pull-up resistors for each open drain output to prevent possible contention between output drivers.

**Note:** In JTAG boundary Scan test mode, all I/Os operate as push/pull drivers and cannot be treated as open drain.

**Table 4** Open Drain I/Os

Signal Name	Ball Number	Comment
RX_LOS_INT	P19	External pull-up resistor of 4.7k $\Omega$ required for proper operation
TX_FAULT_INT	P23	External pull-up resistor of 4.7 k $\Omega$ required for proper operation
MOD_DEF_INT	N22	External pull-up resistor of 4.7 k $\Omega$ required for proper operation
TX_DISABLE_3:0	AA14, AD16, AA7, AB3	External pull-up resistor of 4.7 k $\Omega$ required for proper operation. It is usually resident in optical module (check with the vendor)
UPX_RDY_L	M1	External pull-up resistor of 4.7 k $\Omega$ required for proper operation
I <sup>2</sup> C_DATA_3:0	P24, N24, M24, L24	Bi-directional I/O. Pull-up resistor of 4.7 k $\Omega$ required for proper operation
MDIO	V21	Bi-directional I/O. Pull-up resistor of 4.7 k $\Omega$ required for proper operation
<b>Note:</b> Refer to the Cortina Systems <sup>®</sup> IXF1104 Quad-Port Gigabit Ethernet Media Access Controller (IXF1104 MAC) Datasheet for a complete ball list.		

## 2.10 Boundary Scan (JTAG) Interface

The IXF1104 MAC provides a standard JTAG test port for the boundary scan interface. It consists of these five signals:

- TMS
- TDO
- TDI
- TCK
- TRST\_L

These balls must be terminated correctly for proper device operation. Table 5 lists the Cortina recommended JTAG signal terminations for normal IXF1104 MAC operation.

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**Table 5 Recommended JTAG Termination**

Signal	Required Termination
TRST_L <sup>1,2</sup>	Pull-down through 10 kΩ resistor
TDO	Pull-up through 10 kΩ resistor
TDI	Pull-up through 10 kΩ resistor
TMS	Pull-up through 10 kΩ resistor
TCK	Pull-up through 10 kΩ resistor
<ol style="list-style-type: none"><li>1. If the boundary scan logic is not used, TRST_L must be pulled Low to ensure proper IXF1104 MAC operation. When TRST_L is Low, the JTAG interface is disabled.</li><li>2. If the boundary scan logic is used, TRST_L must be pulled Low after power-up to ensure reset of the Test Access Port (TAP) controller. For more information, refer to the IEEE 1149.1 Boundary Scan Specification.</li></ol>	

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## 3.0 Power and Ground Design

### 3.1 PCB Power Planes

The IXF1104 MAC requires 1.8, 2.5, and 3.3 VDC voltages that are supplied through low-resistance power planes. For the power PCB plane, Cortina recommends the following:

- Use a 0.5 oz. minimum copper power PCB plane thickness
- The 1.8 V and 2.5 V power planes feed RC filter networks that provide power to the analog power balls.
  - Place the filter components close to their respective analog power balls and connect through a greater than 10-mil trace.
  - Keep the CB traces connecting the filter network components as short as possible.

The PCB ground planes provide a low-resistance return path for high-speed switching currents. For the ground PCB plane, Cortina recommends the following:

- Use a 0.5 oz. minimum copper ground PCB plane thickness.
- Avoid multiple ground references (split ground planes) or copper voids due to closely spaced vias, high-density through-hole connectors, fine pitch BGAs, or large board cutouts (slots).
- Minimize PCB layers. Multiple power supplies can coexist on the same layer, provided suitable spacing and isolation are furnished.

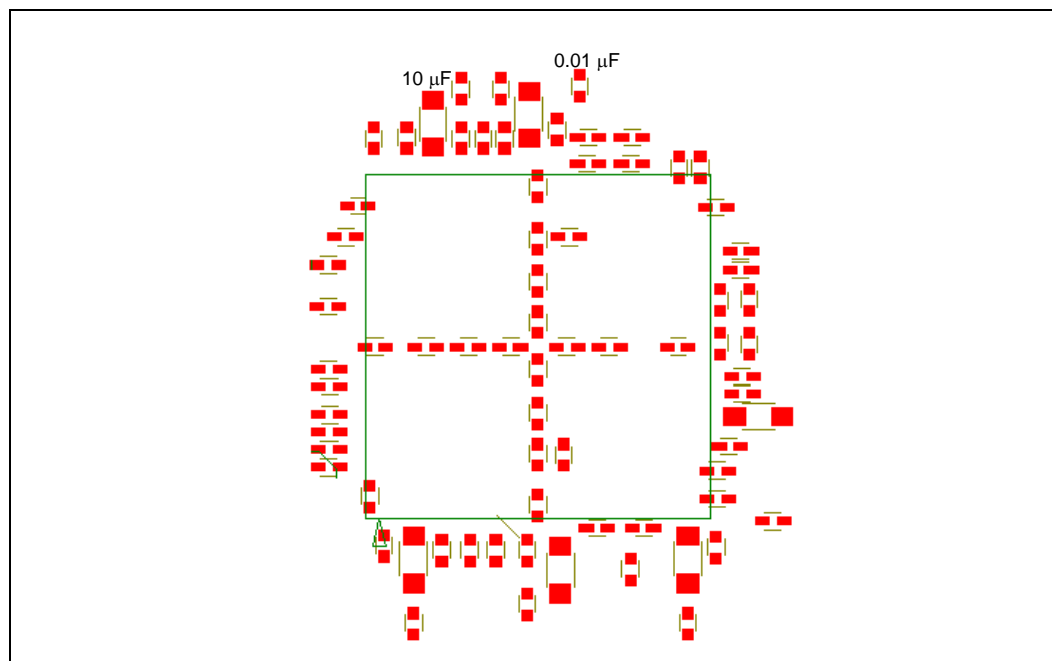
### 3.2 PCB Decoupling Capacitors

Each power supply voltage must have bulk and high-frequency decoupling capacitors. Cortina recommends the following capacitors:

- 10  $\mu\text{F}$  Tantalum for bulk capacitors distributed across the board
- 0.1  $\mu\text{F}$ , 0.01  $\mu\text{F}$ , and 0.001  $\mu\text{F}$  high-frequency ceramic capacitors, placed as close as possible to the BGA power ball

Figure 4 illustrates a typical placement of decoupling capacitors.

**Figure 4** Typical MAC Decoupling Capacitor Placement



### 3.3 Power Supply Sequencing

The power-up and power-down sequence described in this section must be followed to ensure correct IXF1104 MAC operation. The sequence described in this section covers digital and analog power supplies for the IXF1104 MAC.

**Caution:** Failure to follow the sequence described in this section might damage the IXF1104 MAC.

#### 3.3.1 Power-Up Sequence

**Caution:** If the 2.5 V power supplies exceed the 1.8 V power supplies by more than 2.0 V during power-up or power-down, damage can occur to the ESD structures within the analog I/Os. Refer to the Cortina Systems® IXF1104 4-Port Gigabit Ethernet Media Access Controller Datasheet for complete information.

The power-up sequence is as follows:

1. Apply the 1.8 V analog and digital power supplies and verify that they are stable.
2. Apply the 2.5 V analog and digital power supplies.
3. Apply the 3.0 V power supply.

**Note:** The 3.3 V power supply can be powered at any time during the power-up sequence.

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### 3.3.2 Power-Down Sequence

The power-down sequence is the reverse of the power-up sequence.

**Caution:** If the 2.5 V supplies exceed the 1.8 V supplies by more than 2.0 V during power-up or power-down, damage can occur to the ESD structures within the analog I/Os. Refer to the Cortina Systems® IXF1104 Quad-Port Gigabit Ethernet Media Access Controller (IXF1104 MAC) Datasheet for complete information.

The power-down sequence is as follows:

1. Remove the 3.3 V analog and digital power supplies.
2. Remove the 2.5 V analog and digital power supplies.
3. Remove the 1.8 V analog and digital power supplies.

**Note:** The 3.3 V power supply can be removed at any time during the power-down sequence.

## 4.0 Interfaces

This section describes the following four major IXF1104 MAC high-speed interfaces:

- Section 4.1, *SPI3*
- Section 4.2, *RGMI*
- Section 4.3, *GMI*
- Section 4.4, *SerDes*

### 4.1 SPI3

The SPI3 interface consists of a data path and a Tx FIFO status signal.

#### 4.1.1 Data Path

The RX and TX interfaces operate independent of each other. The data path length, however, must be matched with the clock length to ensure set-up and hold timing requirements. To obtain one gigabit on all four ports in MPHY mode, the data path must run at a 133 MHz clock rate. To obtain one gigabit on each port in SPHY mode, each SPI3 interface must run at a 125 MHz clock rate.

The signals have these characteristics:

- 3.3 V LVTTTL interface
- Capable of running between 104 and 133 MHz
- Clocked on the rising edge of the associated clock.

**Note:** Ensure that all timing requirements for data sent to and from the MAC are met.

Refer to the Cortina Systems® IXF1104 Media Access Controller SPI3 Performance Application Note for additional information on SPI3 interface performance.

Table 6 lists the data path signals.

**Table 6** Data Path Signals

Data Path	Transmit	Receive
Clock	TFCLK	RFCLK
Control Signals	TERR_3:0 TENB_3:0 TSOP_3:0 TEOP_3:0 TPRTY_3:0 TMOD[1:0] TSX	RERR_3:0 RVAL_3:0 RSOP_3:0 REOP_3:0 RPRTY_3:0 RMOD[1:0] RSX RENB_3:0
32-bit Data Bus	TDAT[31:0]	RDAT[31:0]
<b>Note:</b> These signals are single-ended 3.3 V LVTTTL.		

### 4.1.2 FIFO Status Signals

The FIFO status path is comprised of a receive and transmit FIFO status path. The two FIFO status paths operate independently. [Table 7](#) lists the SPI3 FIFO status path signals.

**Table 7** SPI3 FIFO Status Signals

Status Path	Transmit
FIFO Control	DTPA_3:0 STPA PTPA TADR[1:0]
<b>Note:</b> These signals are single-ended 3.3 V LVTTTL.	

### 4.1.3 SPI3 PCB Routing

Layout of the SPI3 high-speed signals minimize PCB signal propagation differences between traces. These PCB trace skews are minimized by designing SPI3 traces according to the following constraints:

- Match all RX output signal trace lengths closely (see [Table 8](#)).
- Match all TX input signal trace lengths closely (see [Table 8](#)).
- Ensure setup and hold time requirements are met at each SPI3 device.
- Run all traces above a fixed, solid-ground plane that is continuous across the length of the traces.
- Implement all traces as 50  $\Omega$  micro-strip-type traces.
- In a transmission trace, include a 50  $\Omega$  series termination close to the source output drivers.

All SPI3 PCB traces are designed to the specifications listed in [Table 8](#).

**Table 8** SPI3 PCB Trace Specifications

Specification	Min	Max
Trace Width (w)	4 mil	–
Trace Impedance	50 $\Omega$	–
Trace Difference	–	500 mil

## 4.2 RGMII

The RGMII interface consists of the following:

- 4-bit data bus
- clock
- control line

All of the signals are single-ended, 2.5 V CMOS (3.3 V compatible). This interface is a source-synchronous Double Data Rate (DDR) operating at 125 MHz.

Routing of RGMII signals can occur on any PCB trace layer with the following constraints:

- Implement TX\_CTL\_3:0 and TD[3:0]\_3:0 RGMII output signals as 50  $\Omega$  impedance PCB traces. These traces include series termination resistors, which must be placed close to the IXF1104 MAC RGMII output drivers. Match all TX\_CTL\_3:0 and TD[3:0]\_3:0 trace lengths to within 300 mil.
- TXC\_3:0 requires an additional 1.5 nsec of trace delay on the PCB. This delay is 9 to 10 inches of PCB trace length plus the length of the longest TD[3:0]\_3:0 trace length.
- Implement RX\_CTL\_3:0, RXC\_3:0, and RD[3:0]\_3:0 input signals as 50  $\Omega$  impedance PCB traces. Design the PCB termination and clock delays as recommended by the connecting physical layer component.

## 4.3 GMII

The GMII interface consists of the following:

- 8-bit data bus
- 2 control bits
- clock

All of the signals are single-ended 2.5 V CMOS (3.3 V compatible) with a clock running at 125 MHz. Route the GMII signals with the following constraints:

- Match all RX signals to within 300 mils.
- Match all TX signals to within 300 mils.
- Transmit traces: include a 50  $\Omega$  series termination close to the source output drivers. These signals are implemented as 50  $\Omega$  impedance PCB traces.
- Receive traces: design the PCB termination as recommended by the connecting physical layer component.

## 4.4 SerDes

The SerDes interface consists of the following:

- A receive and transmit differential pair for packet data
- Clock and data lines used for register access and optical module configuration

All the required terminations are built into the IXF1104 MAC for packet data pads. The RX\_P/N pairs are internally terminated with 100  $\Omega$ . Small Form Factor Pluggable (SFP) optical modules interfacing with these devices require AC rather than DC coupling.

**Note:** The PCB layout must support AC coupling. Most SFP modules have internal AC coupling (refer to the appropriate manufacturer's datasheet).

The IXF1104 MAC can operate in an AC- or DC-coupled environment. Set the TX and RX AC/DC Coupling Selection Register (Addr: 0x780) to reflect the external coupling used on the SerDes interface. In AC coupling mode, the driver sources and sinks current to the transmission path and receiver. In DC-coupling mode, the driver sinks current from the transmission path and the receiver acts as a current source to the transmission path. The TX and RX AC/DC Coupling Selection Register (Addr: 0x780) selects the desired coupling assumption independently for each TX and RX interface of the SerDes ports.

Route the SerDes traces with the following constraints:

- Route the traces as 50  $\Omega$  transmission lines.
- Make the traces of equal length on each differential pair and port to minimize skew.
- Run the traces over a single ground plane to match impedance and minimize common mode to differential mode noise conversion.
- Avoid vias and layer changes in the traces.
- If desired, place the traces between two ground planes to improve shielding. This may cause a performance problem if there is an impedance imbalance between the two planes.

Design all SerDes PCB traces to the specifications listed in [Table 9](#).

**Table 9 SerDes PCB Trace Specifications**

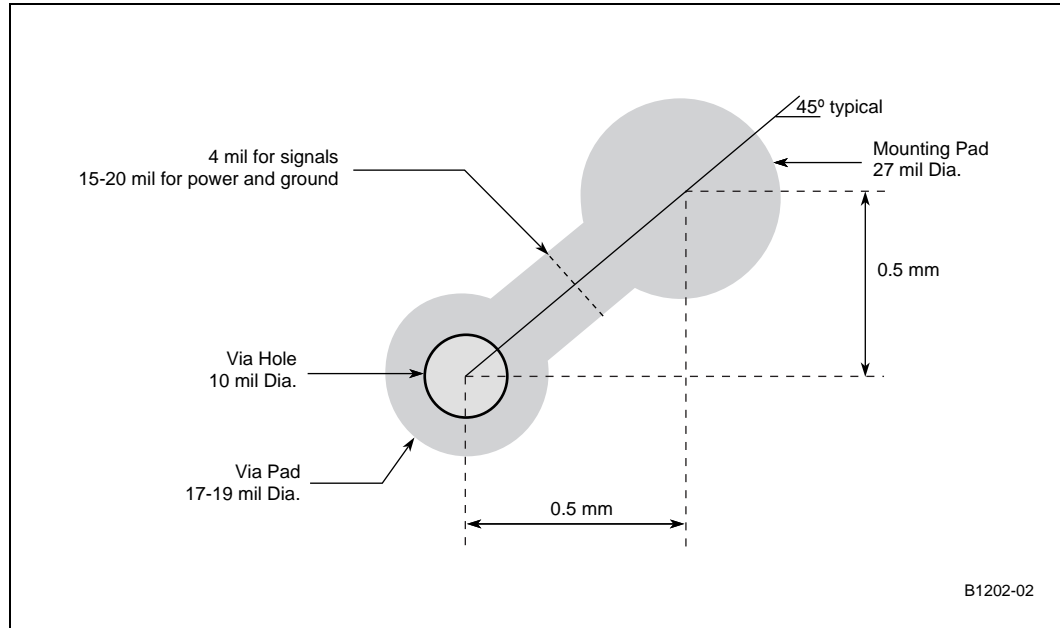
Specification	Min	Max
<b>Trace Width/Impedance</b>		
Trace Width (w)	4 mil	–
Trace Impedance	50 $\Omega$ /100 diff	50 $\Omega$ /100 diff
<b>Trace Separation</b>		
Differential Pair Separation (ds)	4 mil	6 mil
Inter Pair Separation (is)	12 mil	–
<b>Trace Length</b>		
Trace Length Difference	–	100 mil

## 5.0 Device Package Footprint

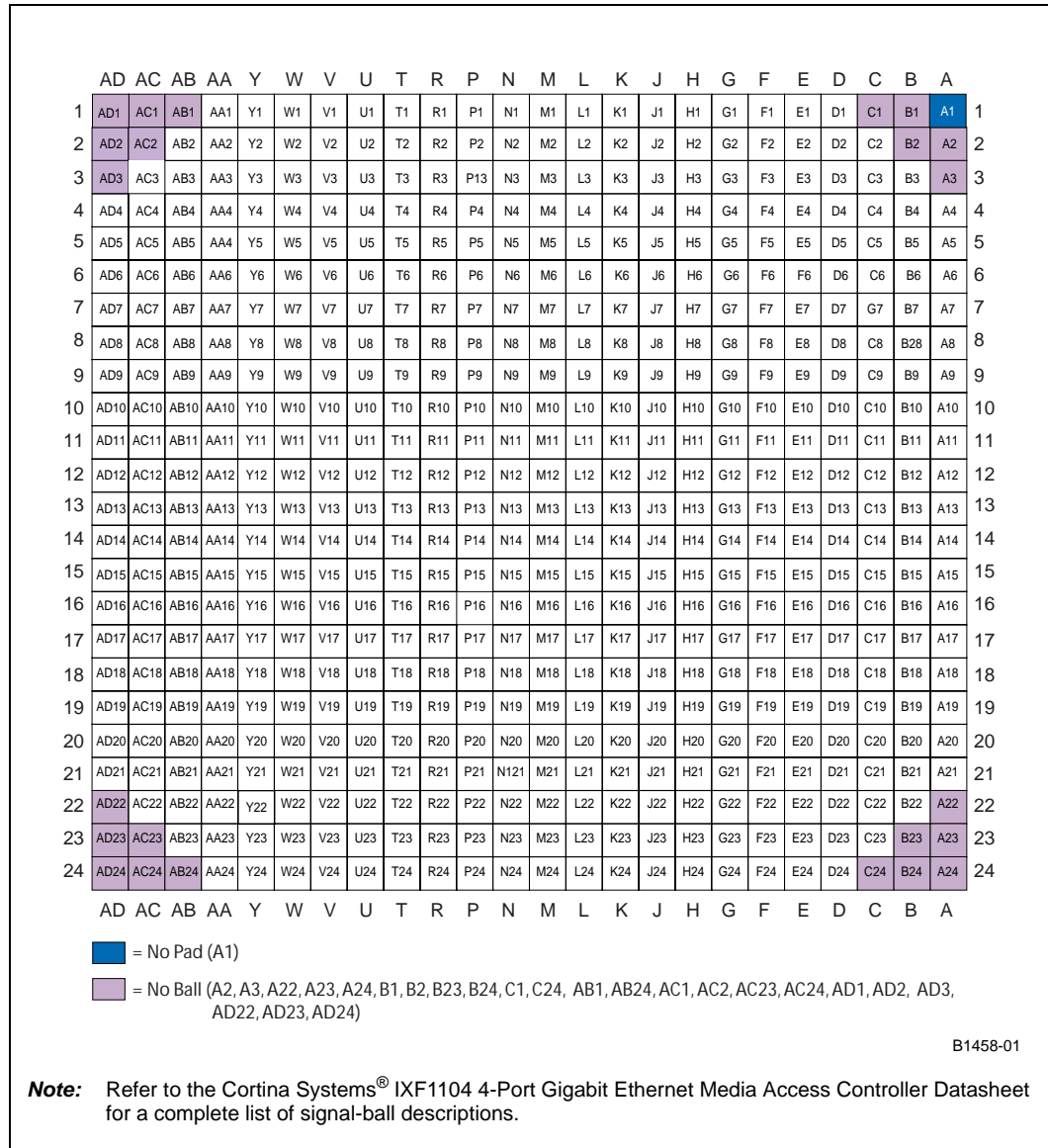
The IXF1104 MAC uses a 552-ball CBGA package, which requires 27 mil BGA landing pads. Mount the package to the PCB with the BGA pad design shown in [Figure 6](#).

**Note:** This CBGA package consists of 576 balls with 6 balls removed diagonally from each corner, for a total of 552 balls used (see [Figure 6](#)).

**Figure 5** 552-Ball CBGA PCB Pad Design



**Figure 6 552-Ball CBGA Ballmap**





**For additional product and ordering information:**

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