



Cortina Systems® IXF1104 Media Access Controller SPI3 Performance

Application Note

12 February 2007

Document Number 280046

Revision 2.0

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Revision History

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| Revision 2.0 Revision Date: 12 February 2007 |
| First release of this document from Cortina Systems, Inc. |

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| Revision 001 Revision Date: July 21, 2004 |
| Initial release. |

1.0 Introduction

The Cortina Systems® IXF1104 Media Access Controller (IXF1104 MAC) implementation of the SPI3 interface is a performance enhancement of the OIF-SPI3-01.0 specification and allows for the additional bandwidth requirement of four ports supporting Gigabit Ethernet. This document discusses those parameter modifications and their effects on applications using the IXF1104 MAC.

1.1 Key Terms

Table 1 Key Terms

| Term | Meaning |
|-------------|--|
| SPI3 | System Packet Interface Level 3 |
| OIF | Optical Interface Forum |
| MPHY | Multiple PHY (32 bit data bus) |
| SPHY | Single PHY (8 bit data bus) |
| Round Robin | Repetitive Sequence |
| MAC | Media Access Controller |
| NPU | Network Processor Unit |
| Pause Cycle | Control Packet requesting pause of data transmission |
| Burst | Continuous data stream of defined duration |

2.0 OIF-SPI3-01.0

2.1 General Description

The OIF-SPI3-01.0 standard defines a packet-based interface for SONET/SDH Physical Layer devices. It is a point-to-point interface running at a maximum 104 MHz operating with either a SPHY 8-bit or a MPHY 32-bit wide interface.

The SPI3 interface uses out-of-band signaling to define packet boundaries, error conditions, packet status, and FIFO status allowing the transfer of control information without impacting traffic data rate across the interface.

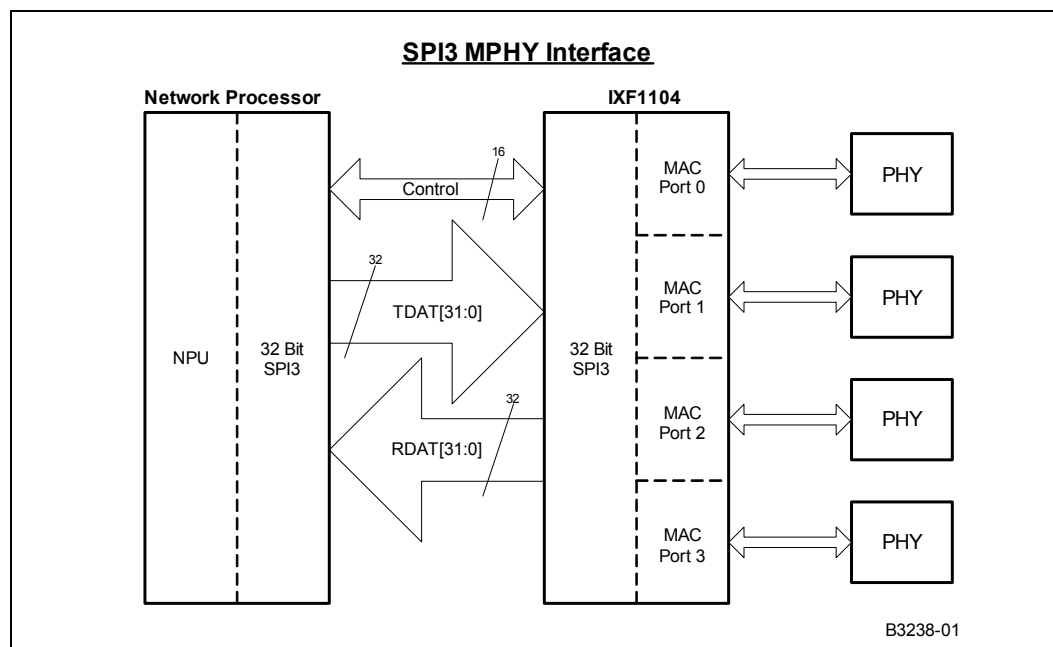
2.2 MPHY

In Multi-PHY (MPHY) mode, the IXF1104 MAC SPI3 interface uses a single 32-bit bus structure and can service up to four line interfaces. (Sharing the SPI3 interface among several ports reduces the number of control and status signals compared to the overhead of four ports in Single-PHY (SPHY) mode, but it requires in-band port addressing to route data packets to and from the correct ports.) The out-of-band signals (RSX and TSX) indicate that port address information is presently on the data bus.

Data received from the line side is transferred to the SPI3 interface in bursts of 64, 128, or 256 bytes using a round-robin algorithm in a continuously repeated cycle. The programmable burst size is the same for all four ports, based on the setting for Port 0 in the SPI3 Receive Configuration register (0x701).

The external Network Processor (NPU) controls transmitted data flow. To select the port, the NPU inserts address information on the data bus and uses the TSX signal to indicate that port addressing information is on the data bus. [Figure 1, SPI3 MPHY Interface](#) illustrates the SPI3 MPHY interface.

Figure 1 SPI3 MPHY Interface



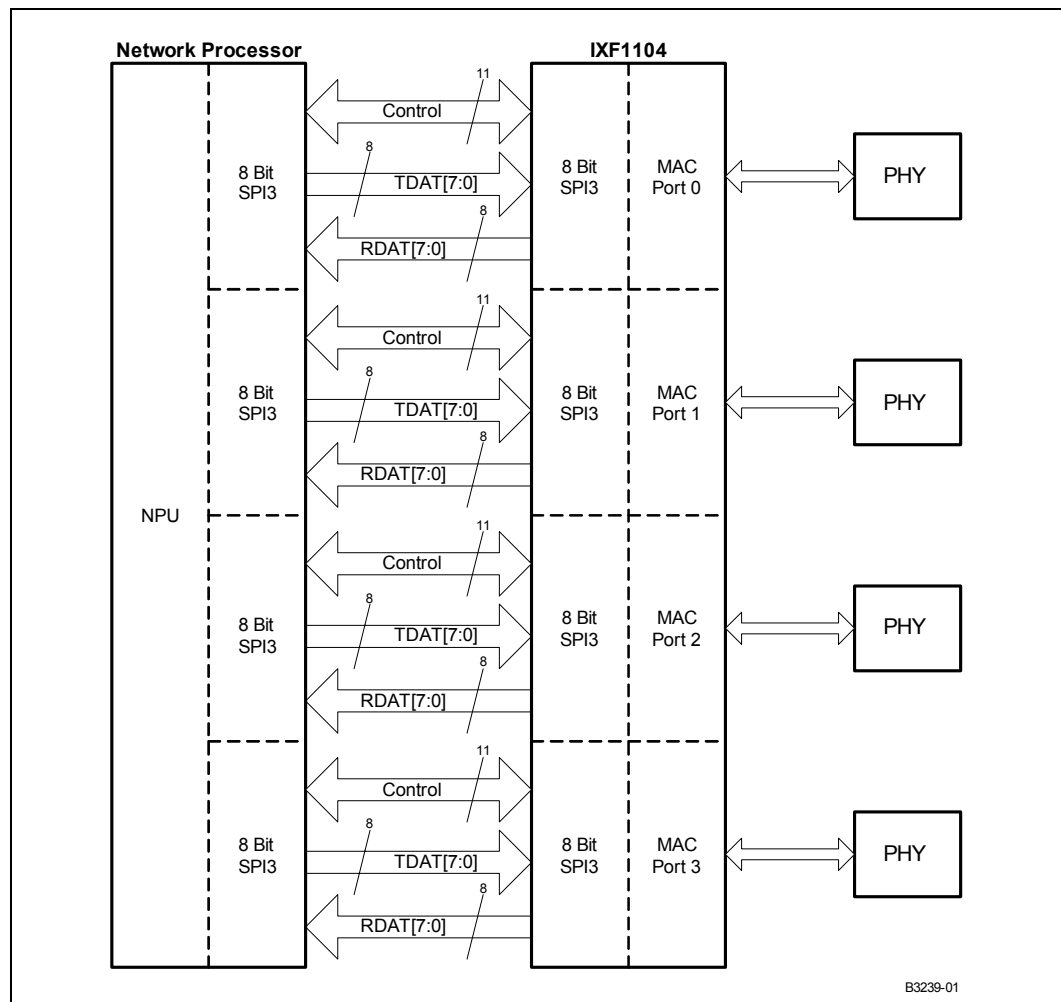
2.3 SPHY

The Single-PHY (SPHY) interface is organized as four, 8-bit buses, each servicing a single MAC port within the IXF1104 MAC. Each SPI3 interface has its own set of control and status signals which increases the routing requirement compared to MPHY, but allows for independent channels.

The data path is for data transfer only (no in-band addressing). Every clock cycle is occupied with packet data directly to and from the line interface.

The IXF1104 MAC allows burst size to be individually configured for each port in SPHY mode. However, this setting takes affect only when the IXF1104 MAC inserts two pause cycles between bursts of 64, 128, or 256 bytes. [Figure 2, SPI3 SPHY Interface](#) illustrates the SPI3 SPHY interface.

Figure 2 SPI3 SPHY Interface



3.0 SPI3 Clock Rates

3.1 Clock and Data Rate

3.1.1 MPHY

The data path is fixed at a 32-bit width in MPHY mode; however, the following parameters affect the overall data rate:

- Number of ports used
- Burst size (from SPI3 Receive Configuration 0x701)
- Reference clock speed

The following equation calculates the data rate in MPHY mode:

Equation 1 $\text{Data Rate} = [\text{Burst} \times 32 \times \text{Reference Clock}] / [(\text{Burst} + 4) \times \text{Number of Ports}]$

The allowed burst sizes for transferring data are 64, 128, and 256 bytes. A single clock cycle between bursts is used for port addressing. This clock cycle occupies the entire bus width of four bytes even though only two bits are used for the actual addressing. Only the number of enabled ports need to be calculated.

Use the following equation to calculate the clock rate for a specific data speed:

Equation 2 $\text{Reference clock} = [(\text{Burst} + 4) \times \text{Number of Ports} \times \text{Data Rate}] / [\text{Burst} \times 32]$

The equations above show that the lower clock rates can support full-line rate when using fewer than four ports. However, the minimum clock that can be used on the SPI3 interface is 88 MHz.

Caution: Clock speeds slower than 88 MHz do not meet IXF1104 MAC internal timing requirements and may result in data errors. The maximum clock speed is 133 MHz.

3.1.2 SPHY

The following is the data rate versus clock speed calculation for SPHY mode:

Equation 3 $\text{Reference Clock} \times 8 = \text{Data Rate}$

The clock speed is 125 MHz for a 1 Gbps rate regardless of the number of ports enabled.

All control and status information is transferred across sideband signals and requires no additional bandwidth. When the B2B_PAUSE bit in the SPI3 Receive Configuration register (0x701) is configured to allow 0 pause cycles between bursts, every clock cycle is occupied with valid data.

3.2 Clock Rate and Layout Issues

3.2.1 SPI3 Specification

The OIF-SPI3 specification defines an interface with the following parameters:

- Maximum output propagation delay = 6.0 ns
- Load requirement = 30 pF (combined capacitor load)
- Maximum clock frequency = 104 MHz

When the IXF1104 MAC operates at 104 MHz, it meets the OIF-SPI3 specification with the following data rates across the SPI3:

- 3.2 Gbps for all four ports in MPHY mode
- 832 Mbps for each port in SPHY mode

The IXF1104 MAC allows overclocking up to 133 MHz to support a 1 Gbps line rate. However, the higher clocking speed requires other parametric modifications, discussed in [Section 3.2.2, SPI3 Application](#) and [Section 3.2.3, PCB Trace Consideration](#).

3.2.2 SPI3 Application

Gigabit Ethernet rates require higher data rates than specified by OIF-SPI3-0.1. The IXF1104 MAC can be overclocked up to 133 MHz to support higher data rates as follows:

- A maximum of 4.25 Gbps total for all ports in MPHY mode
- 1.06 Gbps for each port operating in SPHY mode.

Higher clock rates mean faster clock and data edges and shorter clock periods. The OIF specification requires modification for SPI3 operation at 133 MHz. The following are the affected parameters:

- Maximum output propagation delay = 3.7 ns
- Load requirement = 20 pF (combined capacitor load)
- Maximum external clock input frequency = 133 MHz

The propagation delay and the 20 pF load requirement are interrelated. Internally, the IXF1104 MAC meets the 3.7 ns propagation delay. However, capacitance on the output slows the rising and falling edges of data and clock signals. Output capacitance loads greater than 20 pF retard the rise and fall times enough to impact the ability of the IXF1104 MAC to meet the 3.7 ns requirement.

Note: The output capacitance requirement is a test specification and has minimal impact on the layout (refer to [Section 3.2.3](#)).

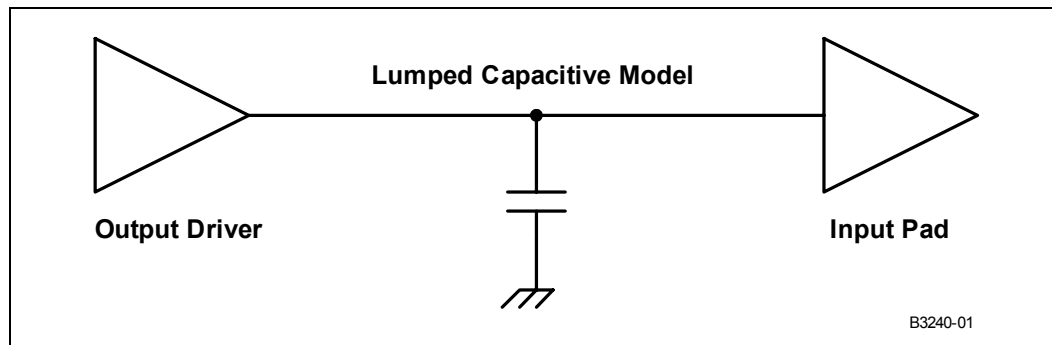
3.2.3 PCB Trace Consideration

Despite the lower capacitive load requirement for operation at 133 MHz, the IXF1104 MAC SPI3 interface traces can be implemented using a standard high-speed controlled impedance PCB design.

In the OIF-SPI3-0.1 specification, the output load is specified as a lumped capacitive load (see [Figure 3, Lumped Capacitive Model](#)).

The model shown in [Figure 3](#), *Lumped Capacitive Model* is a test specification and so does not accurately represent a transmission line. The purely capacitive load lacks series inductance or resistance and the output driver drives the capacitance directly.

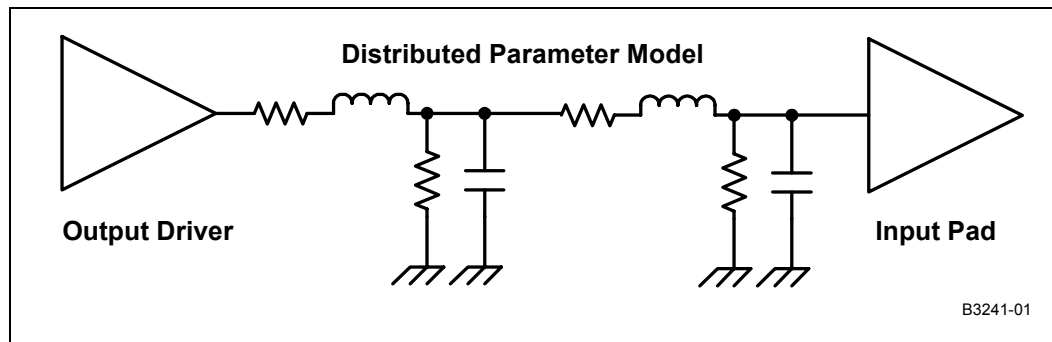
Figure 3 Lumped Capacitive Model



[Figure 4](#) shows a more accurate and commonly used transmission-line model. This example has only two segments but longer traces would involve a greater number of segments and various configurations. In any case, the total combined equivalent capacitive load cannot exceed 20 pF.

The model in [Figure 4](#) shows that capacitance is distributed along the transmission line and is separated by resistive and inductive elements. The number of segments and the element values are determined by the length and characteristics of the transmission line.

Figure 4 Distributed Parameter Model



Using the [Figure 4](#) model, and in real world applications, the IXF1104 MAC drivers do not drive a capacitive load directly as specified in the OIF-SPI3 specification. Instead, the driver sees a lower capacitive value through series resistance or inductance, allowing the output to slew at rates that permit a propagation delay of 3.7 ns or less.

The distributed parameter model meets the required performance for operation at 133 MHz using common high-speed PCB transmission line design guides.

4.0 Conclusion

The IXF1104 MAC may require overclocking to meet Gigabit Ethernet speeds on all ports. Overclocking is not necessary under the following circumstances:

- In some Gigabit applications with three or fewer ports when the SPI3 is configured for MPHY mode.
- In applications implementing only Fast Ethernet (10/100 Mbps).

Impedance-controlled PCB traces using common high-speed trace design methodology should be sufficient when overclocking is required.

In IXF1104 MAC performance testing, use the 30 pF load only when testing to the OIF-SPI3-01.0 standard at the specified 104 MHz clock. Limit output loads to 20 pF for testing at data rates that require clock rates above the OIF specification.



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