



Cortina Systems[®] LXT9785/LXT9785E Advanced 8-Port 10/100 Mbps PHY Tranceiver

Specification Update

16 April 2007

Document Number 249357

Revision 13.0

*Other names and brands may be claimed as the property of others.

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Revision History

Revision 13.0 Revision Date: 05 March 2007
First release of this document from Cortina Systems, Inc.

Revision Number: 012 Revision Date: March 29, 2006
Modified Table 7, LXT9785/LXT9785E PHY Transceiver Ordering Information .
Modified Figure 4, Ordering Information, on page 12 .

Revision Number: 011 Revision Date: September 16, 2003
Modified "Errata" table.
Added Erratum 11 "LED Stretch" .
Added Erratum 12 "Far-End Fault Reporting" .
Added Erratum 13 "Destination Address in 10 Mbps Mode" .
Added Erratum 14 "Changing Advertised Duplex While Link Is Up" .
Added Erratum 15 "FIFO Error Bit During FIFO Overwrites" .
Added Erratum 16 "SLP Detection in Forced 100 Mbps Mode"
Added Erratum 17 "Detection of Illegal Symbols After SSD" .
Added Erratum 18 "RXD[1:0] Signal in RMII Mode" .
Added Erratum 19 "RMII During False Carrier Event" .
Added Erratum 20 "Receive Error Count Register Incrementing" .
Added Erratum 21 "False Carrier Over-Extension" .
Added Erratum 22 "Power-On-Reset (POR) Configuration Function" .
Added Erratum 23 "Duplex Status and LED Behavior During DTE Discovery" .
Added Specification Clarification 1 " LXT9785/LXT9785E Operating Conditions Table"
Deleted all existing Specification Changes and Documentation Changes from this document and rolled into LXT9785 Datasheet.
Added Documentation Change 1 "BGA15 Twisted-Pair Signal Description Update" .
Added Documentation Change 2 "Cable Diagnostic Behavior In Forced 10BASE-T Mode" .
Modified Documentation Change 3 "Product Ordering Information" .

Revision Number: 010 Revision Date: January 9, 2003
Internal release.



Revision Number: 009 Revision Date: October 3, 2002
Added Errata 8 through 10 to "Errata" table.
Modified chip markings under "Identification Information".
Added Erratum 8: "Establishment of Link in Forced 100 Mbps Mode" to "Errata" section.
Added Erratum 9 "100 Mbps False RXER" to "Errata" section.
Added Erratum 10 "FIFO Lockup" to "Errata" section.
Added "Port Power-Up After Speed Change" to "Documentation Changes".
Modified Table 1, "Product Information" with Fab 5 number changes.
Modified Figure 2, "Ordering Information - Sample" with status of "V".

Revision Number: 008 Revision Date: June 2002
Updated "Errata" table.
Added Erratum 7: "Improper Reset of Internal JTAG Control Flip-Flops" to "Errata" section.
Added "Parallel Detection" to "Documentation Changes" section.
Modified Table 2 "Product Information".

Revision Number: 007 Revision Date: April 2002
Modified Stepping/Revision table: Added C2 information.
Specification Changes: Added Interrupt Enable Register table.
Added Table 28 to Documentation Changes.
Modified Product Ordering table and diagram.

Revision Number: 006 Revision Date: January 24, 2002
Added Errata 5 and 6.
Incorporated Specification Changes 1 through 5 into LXT9785/LXT9785E Datasheet and deleted them from this Specification Update. Rolled Documentation Change into LXT9785/LXT9785E Datasheet.
Modified Product Ordering table.

Revision Number: 005 Revision Date: September 21, 2001
Revised Manufacturer's Revision Number for all steppings in the Stepping table.
Revised Table 1 and Table 2 under Specification Changes.
Revised last paragraph under Specification Changes No. 3.
Specification Changes: FIFO Size Control Pins: Removed last sentence in first para and FIFO Depth table.
Documentation Changes: Revised Product Ordering Information table.



Revision Number: 004 Revision Date: September 14, 2001
Edited Errata, Specification Changes, and Document Changes tables.
Revised "Stepping / Revision" paragraph and "Manufacturer's Revision Number" column in table.
Erratum 1: Removed from Errata and placed in Specification Changes section; replaced problem description; changed status.
Erratum 2: Now Erratum 1; changed status.
Erratum 3: Now Erratum 2; changed status.
Erratum 4: Now Erratum 3; changed status.
Added Erratum4: DTE Discovery Next Page Support
Specification Changes: Added Items 1 through 5.
Added Product Ordering Information

Revision Number: 003 Revision Date: April 6, 2001
Included LXT9785E throughout document
Updated "Markings" table
Added Errata 2 and 3
Added Specification Changes 1
Removed information under Documentation Changes

Revision Number: 002 Revision Date: February 5, 2001
Removed pre-production Stepping Errata.
Updated "Markings" table with Manufacturer's Revision Code information.
Added Errata 1 and 2.
Added Documentation Changes 1, 2, and 3

Revision Number: 001 Revision Date: January 15, 2001
Converted formats (no technical or material changes).

1.0 Preface

This document is an update to the specifications contained in the Affected Documents/ Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

1.1 Affected Documents/Related Documents

Title	Document Number
Cortina Systems® LXT9785/LXT9785E Advanced 10/100 8-Port Transceivers Datasheet	249241
Cortina Systems® LXT9785 Design and Layout Guide	249509

1.2 Nomenclature

Errata are design defects or errors. These may cause the Cortina Systems® LXT9785/ LXT9785E Advanced 8-Port 10/100 Mbps PHY Transceiver's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's life cycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

2.0 Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the LXT9785/LXT9785E PHY Tranceiver. Cortina Systems, Inc. (Cortina) may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

2.1 Codes Used in Summary Table

Stepping

X: Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.

(No mark)

or (Blank box): This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page): Page location of item in this document.

Status

Doc: Document change or update will be implemented.

No Fix: There are no plans to fix this erratum.

Plan Fix: This erratum may be fixed in a future stepping of the product.

Table 1 Errata (Sheet 1 of 2)

No.	Steppings				Page	Status	ERRATA
	1	2	3	4			
1	X				page 13	Fixed	<i>Packet Fragments Caused by Tx FIFO Underflow</i>
2	X				page 13	Fixed	<i>FIFO Size Control</i>
3	X				page 14	Fixed	<i>Software Control of MDI/MDIX</i>
4	X				page 15	Fixed	<i>DTE Discovery Next Page Support</i>
5			X	X	page 15	No Fix	<i>RX FIFO Reserved Setting</i>
6	X	X	X		page 15	Fixed	<i>Internal Loopback Receive Disable</i>
7	X	X	X		page 16	Fixed	<i>Improper Reset of Internal JTAG Control Flip-Flops</i>
8	X	X	X		page 16	Fixed	<i>Establishment of Link in Forced 100 Mbps Mode</i>
9	X	X	X		page 17	Fixed	<i>100 Mbps False RXER</i>
10			X		page 17	Fixed	<i>FIFO Lockup</i>
11	X	X	X		page 18	Fixed	<i>LED Stretch</i>
12	X	X	X		page 18	Fixed	<i>Far-End Fault Reporting</i>
13			X		page 19	Fixed	<i>Destination Address in 10 Mbps Mode</i>
14	X	X	X		page 19	Fixed	<i>Changing Advertised Duplex While Link Is Up</i>

Table 1 Errata (Sheet 2 of 2)

No.	Steppings				Page	Status	ERRATA
	1	2	3	4			
15	X	X	X		page 19	Fixed	<i>FIFO Error Bit During FIFO Overwrites</i>
16		X	X	X	page 20	No Fix	<i>SLP Detection in Forced 100 Mbps Mode</i>
17	X	X	X	X	page 20	No Fix	<i>Detection of Illegal Symbols After SSD</i>
18	X	X	X	X	page 20	No Fix	<i>RXD[1:0] Signal in RMII Mode</i>
19	X	X	X	X	page 21	No Fix	<i>RMII During False Carrier Event</i>
20	X	X	X	X	page 21	No Fix	<i>Receive Error Count Register Incrementing</i>
21	X	X	X	X	page 21	No Fix	<i>False Carrier Over-Extension</i>
22		X	X		page 22	Fixed	<i>Power-On-Reset (POR) Configuration Function</i>
23	X	X	X	X	page 22	No Fix	<i>Duplex Status and LED Behavior During DTE Discovery</i>

Table 2 Specification Changes

No.	Steppings				Page	Status	SPECIFICATION CHANGES
	1	2	3	4			
1							None for this revision of this specification update.

Table 3 Specification Clarifications

No.	Steppings				Page	Status	SPECIFICATION CLARIFICATIONS
	1	2	3	4			
1				X	page 24	Doc	<i>LXT9785/LXT9785E PHY Transceiver Operating Conditions Table</i>

Table 4 Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
1	007	page 25	Doc	<i>BGA15 Twisted-Pair Signal Description Update</i>
2	007	page 25	Doc	<i>Cable Diagnostic Behavior In Forced 10BASE-T Mode</i>

3.0 Identification Information

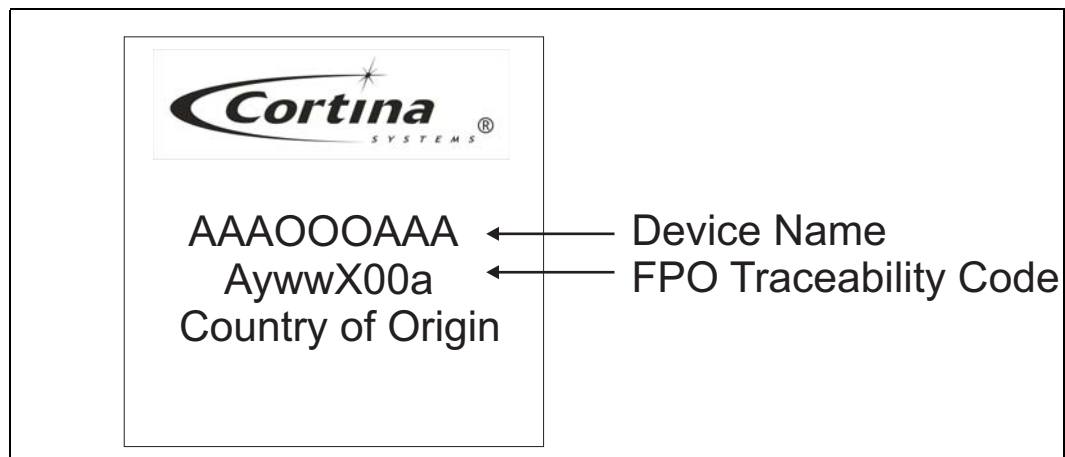
3.1 Markings

Figure 1 shows a sample PBGA package for the LXT9785/LXT9785E PHY Tranceiver (see Section 4.0, *Product Ordering Information*, on page 11 for specific part numbers).

Note: In contrast to the Pb-Free (RoHS-compliant) PBGA package, the non-RoHS-compliant package does not have the “e1” symbol in the last line of the package label.

Note: Further information regarding RoHS and lead-free components can be obtained from your local Cortina representative.

Figure 1 Example of Top Marking Information Labeled as Cortina Systems, Inc.



Earlier versions of the silicon may be marked as either Intel* or Level One Communications* as shown in Figure 2 and Figure 3.

Figure 2 Example of Top Marking Information Labeled as Intel Corporation*

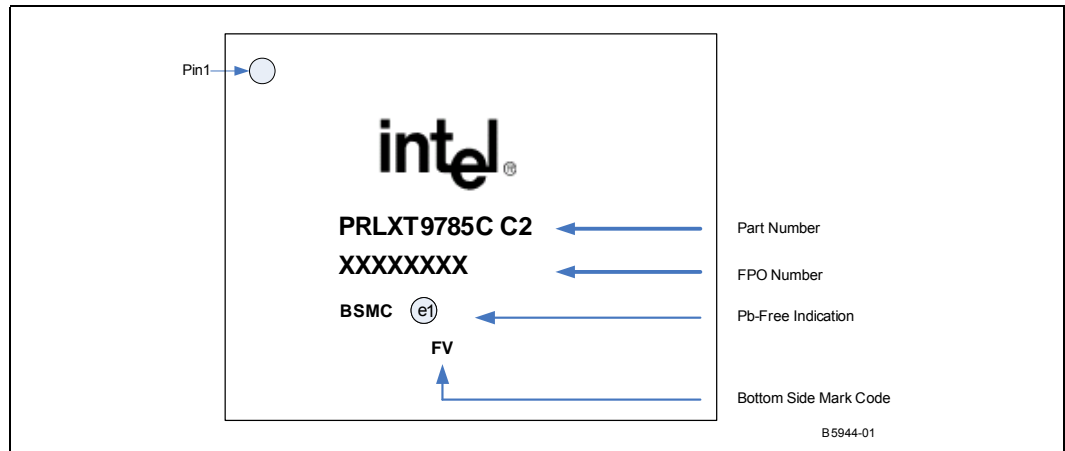
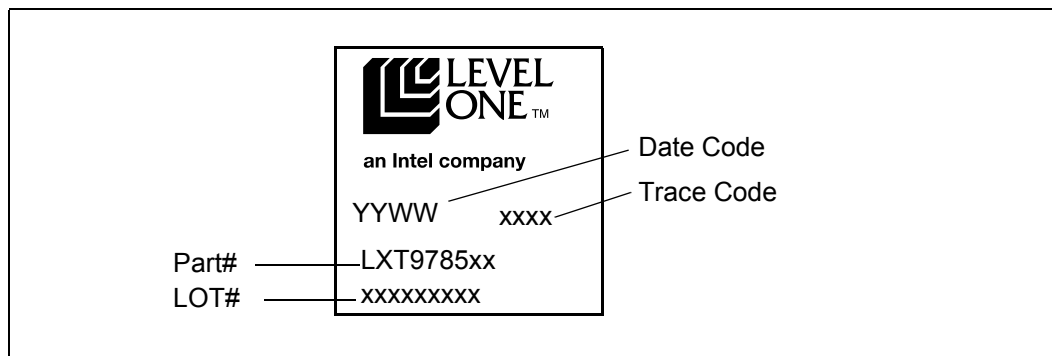


Figure 3 Example of Top Marking Information Labeled as Level One Communications*



3.1.1 Stepping/Revision Numbers

A “Stepping Number” is assigned when any product design update is released that changes the device errata or specification. A “Revision Number” is assigned to each device tapeout, regardless of impact to device errata or specification. The “Manufacturer’s Revision Number” may be read by software from Register 3, bits 3:1 in the LXT9785/LXT9785E PHY Tranceiver.

Table 5 LXT9785/LXT9785E PHY Tranceiver Steppings

Stepping	Revision Number	Trace Codes ¹	Manufacturer’s Revision Number ²	Model Variant ³	Part Number
1	A4	KxDx	001	0	LXT9785
2	B2	N/A	011	0	LXT9785
2 B2		N/A	011	1	LXT9785E
3	C2	N/A	101	0	LXT9785
3	C2	N/A	101	1	LXT9785E
4	D0	N/A	111	1	LXT9785/LXT9785E

1. x indicates an insignificant variable.
 2. This value is from Register bits 3.3:1. Please see the LXT9785/LXT9785E Datasheet for more information.
 3. This value is from Register bit 3.0. Please see the LXT9785/LXT9785E Datasheet for more information.

Table 6 shows a list of JTAG numbers, which vary with steppings and revision numbers:

Table 6 LXT9785/LXT9785E PHY Tranceiver JTAG Numbers

Device	Rev	Version	Part ID	Jedec Cont.	JEDEC ID	Rsvd	Hex
–	–	31:28	27:12	11:8	7:1	0	–
LXT9785/E	D0	1111	0010011000111001	0000	11111110	1	F26390FD
LXT9785	C2	1010	0010011000111001	0000	11111110	1	A26390FD
LXT9785E	C2	1011	0010011000111001	0000	11111110	1	B26390FD
LXT9785	B2	0110	0010011000111001	0000	11111110	1	626390FD
LXT9785E	B2	0111	0010011000111001	0000	11111110	1	726390FD

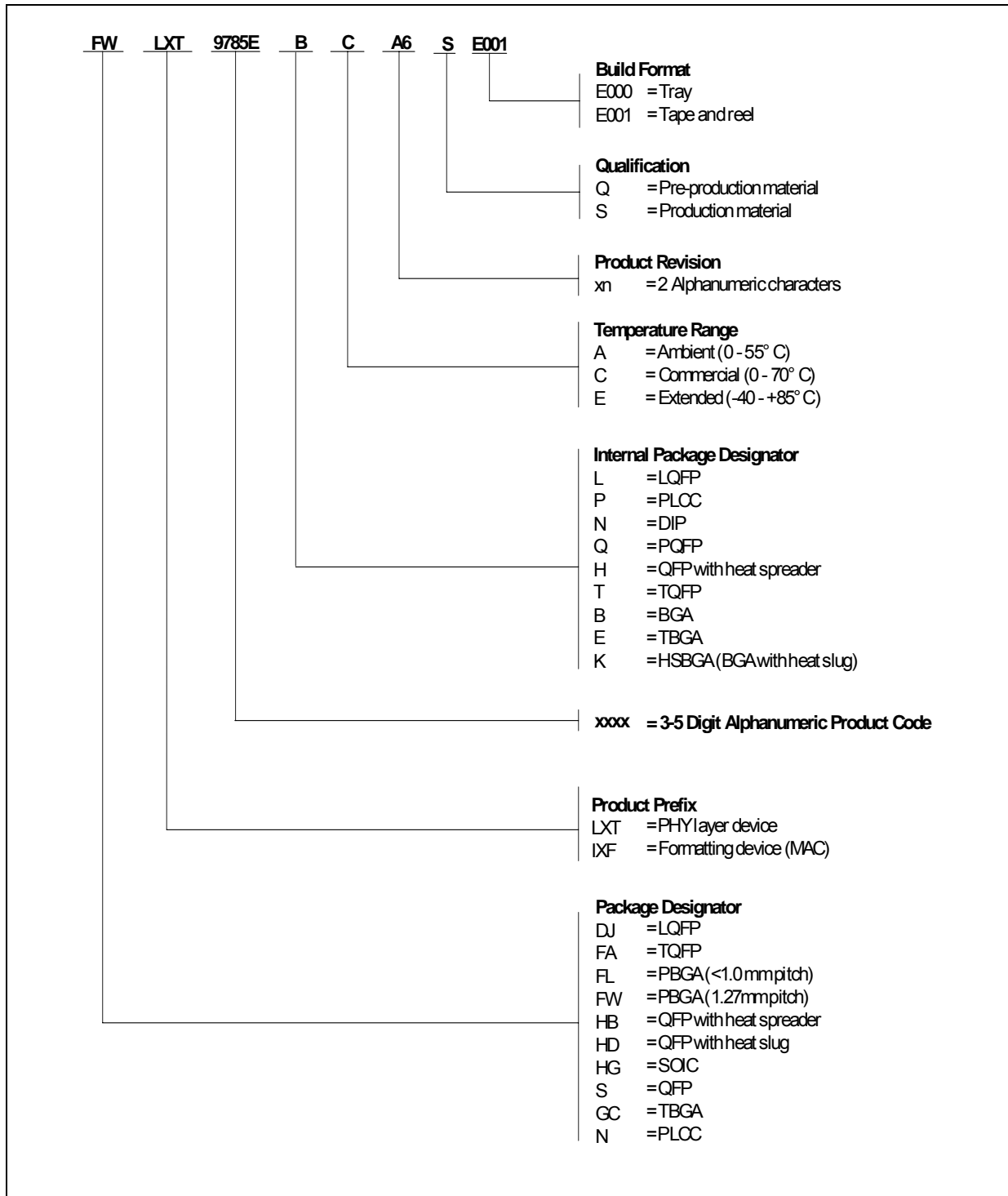
4.0 Product Ordering Information

Table 7 and Figure 4 provide product ordering information.

Table 7 LXT9785/LXT9785E PHY Tranceiver Ordering Information

Number	Revision	Package Type	Pin Count	RoHS Compliant
FWLXT9785BC.D0	D0	PBGA	241	No
PRLXT9785BC.D0	D0	PBGA	241	Yes
FWLXT9785EBC.D0	D0	PBGA	241	No
PRLXT9785EBC.D0	D0	PBGA	241	Yes
FWLXT9785BC.C2V	C2V	PBGA	241	No
PRLXT9785BC.C2V	C2V	PBGA	241	Yes
FWLXT9785EBC.C2V	C2V	PBGA	241	No
PRLXT9785EBC.C2V	C2V	PBGA	241	Yes
GDLXT9785MBC.D0	D0	PBGA	196	No
LULXT9785MBC.D0	D0	PBGA	196	Yes
HBLXT9785HC.D0	D0	HQFP	208	No
WBLXT9785HC.D0	D0	HQFP	208	Yes
HBLXT9785EHC.D0	D0	HQFP	208	No
WBLXT9785EHC.D0	D0	HQFP	208	Yes
HBLXT9785HE.D0	D0	HQFP	208	No
WBLXT9785HE.D0	D0	HQFP	208	Yes
HBLXT9785EHC.C2V	C2V	HQFP	208	No
WBLXT9785EHC.C2V	C2V	HQFP	208	Yes
HBLXT9785HC.C2V	C2V	HQFP	208	No
WBLXT9785HC.C2V	C2V	HQFP	208	Yes
HBLXT9785HE.C2V	C2V	HQFP	208	No
WBLXT9785HE.C2V	C2V	HQFP	208	Yes

Figure 4 Ordering Information



5.0 Errata

Erratum 1: Packet Fragments Caused by Tx FIFO Underflow

Problem The LXT9785/LXT9785E PHY Transceiver transmit (Tx) FIFO may experience an underflow condition due to either jitter or a frequency mismatch on the internal Tx FIFO read and write clocks.

Implication On boards with non-optimal REFCLK or transmit clock signal quality, one port of the LXT9785/LXT9785E PHY Transceiver may occasionally transcend into a state where some 100 Mbps packets are transmitted as fragments and/or with CRC errors.

Workaround **Hardware:** To minimize the potential for this erratum to occur, it is recommended that, in regard to clocking, board designers closely follow Cortina's board-design guidelines in the "Cortina Systems® LXT9785/LXT9785E PHY Transceiver Design and Layout Guide."

Software: To prevent this erratum from occurring, increase the Tx FIFO initial fill level by writing Register bit 16.5 = 1. Note that this software workaround has the following side effects:

- TXEN to TPFO transmit latency increases by 40 ns
- TPFI to CRS asserted receive latency remains unchanged
- CRS asserted to Start-of-Stream Delimiter (SSD) increases from 320 ns to 1280 ns (not specified in the datasheet)
- Preamble is enabled in 10BASE-T mode. Set RX_DV High and RXD = preamble when CRS is asserted

Status Fixed

Erratum 2: FIFO Size Control

Problem Register bit 16.6 does not control the receive (Rx) FIFO depth as documented in the LXT9785/LXT9785E Datasheet (Revisions 001 to 002). In LXT9785/LXT9785E PHY Transceiver Stepping 1, the FIFO depth control is tied to the Preamble Enable Register bit 16.5.

Implication Writing Register bit 16.6 = 0 or Register bit 16.6 = 1 has no effect on the transceiver's functionality.

Workaround Increasing the FIFO depth allows the LXT9785/LXT9785E PHY Transceiver to support Jumbo (9 KByte) packets with a large frequency variation on the local reference clock and remote clock from the link partner. The formula to determine the maximum packet size supported is as follows:

Maximum packet size (Bytes) =
Rx FIFO depth (Bytes) / (2 x (local frequency tolerance + remote frequency tolerance))

Example: Maximum packet size (Bytes) = 4 / (2 x [100 + 1000] / 10⁶) = 1818 Bytes
assuming a 4 Byte default Rx FIFO depth, 100 ppm local frequency tolerance, and
1000 ppm remote frequency tolerance

In LXT9785/LXT9785E PHY Transceiver Stepping 1, the FIFO depth can be increased with Register bit 16.5. The affects of Register bit 16.5 are shown in the following chart:

Function	16.5 = 0	16.5 = 1
10BASE-T Preamble	disabled	enabled
Rx FIFO depth	4 Bytes	16 Bytes
Tx FIFO depth	4 bits	8 bits

Writing Register bit 16.5 = 1 causes the PHY to have the following behaviors:

- TXEN to TPFO transmit latency increases by 40 ns
- TPF1 to CRS asserted receive latency remains unchanged
- CRS asserted to Start-of-Stream Delimiter (SSD) increases from 320 ns to 1280 ns (not specified in the datasheet)
- Preamble enabled in 10BASE-T mode; set RX_DV High and RXD = preamble when CRS is asserted

Status Fixed

Erratum 3: Software Control of MDI/MDIX

Problem The Tx/Rx polarity on one or more ports could be set incorrectly despite the setting of the Manual MDI/MDIX Register bit 27.8. This condition could occur if the hardware MDI/MDIX or auto MDI/MDIX configuration registers change within 30 μ s of the LXT9785/LXT9785E PHY Tranceiver recovering from reset or when consecutive MDI/MDIX register changes occur in less than 30 μ s.

When the MDI/MDIX state changes, either due to the auto MDI/MDIX algorithm or a change to Register bits 27.9:8, the polarity change is performed in stages. The internal MDI/MDIX state machine has a 30 μ s counter that is initiated by a random number generator associated with the PHY and port addresses. When the counter reaches 12 μ s, it reads Register bits 27.9:8 to determine the desired MDI/MDIX state. If the MDI/MDIX register setting is changed when the counter is between 12 μ s and 30 μ s, the change is not recognized.

Implication This erratum occurs only if the MDI/MDIX mode is changed via software. If it does occur, this erratum would likely show up on only one or a few ports because the MDI/MDIX state machine counter is initiated at a different random time on each port. The probability of occurrence depends on coincidental timing between software writing to the register and when the internal state machine counter values are within a specific range.

Workaround **Hardware:** This erratum can be prevented by setting the hardware configuration to the desired MDI, MDIX, or auto MDI/MDIX mode. Use the following hardware settings.

- **MDI mode**
AMDIX_EN pin 83/ball K1 = *inactive Low* and MDIX pin 59/ball D2 = *inactive Low*
- **MDIX mode**
AMDIX_EN pin 83/ball K1 = *inactive Low* and MDIX pin 59/ball D2 = *active High*
- **Auto MDI/MDIX mode**
AMDIX_EN pin 83/ball K1 = *active High* and MDIX pin 59/ball D2 = *don't care*

Software: If the ability to change the MDI/MDIX mode in software is desired, perform the following procedure to prevent this erratum from occurring.

1. After reset, disable auto MDI/MDIX and set the Manual MDIX register bit to the *opposite* of the desired mode. For example, if MDIX mode is ultimately desired, write Register bits 27.9:8 = 00.

If MDI mode is ultimately desired, write Register bits 27.9:8 = 01.

2. Wait at least 30 μ s.
3. Rewrite to the Manual MDIX register the desired state. For example, if MDIX mode is desired, write Register bits 27.9:8 = 01. If MDI mode is desired, write Register bits 27.9:8 = 00.

This procedure helps ensure that a state change occurs, which initiates the MDI/MDIX state machine. It also allows enough time between state changes for the internal MDI/MDIX state machine counter to time-out and accept new changes to Register bit 27.8.

Status Fixed

Erratum 4: DTE Discovery Next Page Support

Problem The LXT9785/LXT9785E PHY Tranceiver will not complete auto-negotiation under the following conditions:

- DTE Discovery Mode Enabled (Register bit 27.6 = 1)
- Link Partner supports Next Pages
- Link Partner sends less than 5 non-null code Next Pages

Implication The LXT9785/LXT9785E PHY Tranceiver will not establish link nor indicate that a non-phone link partner has been detected when it is in the above configuration.

Workaround There is no work around for this problem.

Status Fixed

Erratum 5: RX FIFO Reserved Setting

Problem Setting Register bit 18.15 = 1 and Register bit 18.14 = 1 to increase RX FIFO size to 16 bytes is incompatible with the RMII interface. The CRS_DV signal stays High during IPG in RMII mode instead of transitioning to Low, as in SMII and SS-SMII modes.

Implication CRC errors will occur.

Workaround Use RX FIFO depths of eight or fewer bytes in RMII mode.

Status No Fix

Erratum 6: Internal Loopback Receive Disable

Problem The recovered clock from the receive data is used instead of the transmit clock when setting a port to 10 Mbps internal loopback mode.

Implication When the port is connected to a link partner transmitting data or idle signals, the loopback data is corrupted because the receiver data recovered clock is used to capture the loopback data.

Workaround Clear Register bit 16.8 so that the proper clock is used. This bit is set on power-up.

Status Fixed

Erratum 7: Improper Reset of Internal JTAG Control Flip-Flops

Problem Power-on cycling may cause the LXT9785/LXT9785E PHY Tranceiver to come out of reset in an unknown state due to the improper reset of some internal JTAG control flip-flops.

Implication Some internal JTAG flip-flops may not be reset properly, which can cause the input and output steering muxes to be selected incorrectly.

Workaround Use the following options for a workaround:

- Designs not currently using JTAG should tie the TRST pin directly to ground.
- Designs using the four-signal option and not using the TRST pin for reset should use a 10 k Ω to 12 k Ω pull-down resistor from the TRST pin to ground.
- Designs using the five-signal option should tie the TRST pin to ground through a resistor. The suggested value of the resistor may be determined by $V_{ol\ max}/I_{il\ max}$. (For example, $0.5\ V / 500\ \mu A = 1.0\ k\Omega$, where 0.5 V is the maximum allowable logic low level presented to the LXT9785/LXT9785E PHY Tranceiver TRST pin, and 500 μA is the maximum sink current provided by all devices connected in parallel at the TRST pin).
- Designs using the five-signal option with a determined resistor value of $<1\ k\Omega$ should use a buffer to drive the TRST pin and provide a Low-to-High signal after reset. The suggested buffer should be capable of driving the TRST pin Low, then High while maintaining the proper logic levels.

Status Fixed

Erratum 8: Establishment of Link in Forced 100 Mbps Mode

Problem Link may not come up reliably when the following occurs:

- The LXT9785/LXT9785E PHY Tranceiver is in forced 100 Mbps mode and link is down.
- The link partner is configured to auto-negotiate.
- The link partner cannot handle instantaneous jitter on the MLT3 signal during link-up.

Implication If this condition occurs, communication between the LXT9785/LXT9785E PHY Tranceiver and its link partner may not establish. This condition does not occur in other LXT9785/LXT9785E PHY Tranceiver speed-setting combinations.

Workaround Configure the LXT9785/LXT9785E PHY Tranceiver for auto-negotiation rather than forced 100 Mbps mode, or configure the link partner to forced 100 Mbps instead of auto-negotiation to establish link.

Status Fixed

Erratum 9: 100 Mbps False RXER

Problem If an errored packet is received in 10 Mbps mode and a 100 Mbps speed change is made before receiving another good 10 Mbps packet, the LXT9785/LXT9785E PHY Tranceiver may assert RXER (Receive Error) on the out-of-band signaling and increment the RXER counter (Register 21) for every packet received in 100 Mbps mode. This is independent of speed selection (auto-negotiation or forced speed).

Implication All 100 Mbps received packets will be flagged with an error on the out-of-band signaling and Register 21 will be incremented.

Workaround Workaround 1:

Part A: Use the following sequence if the LXT9785/LXT9785E PHY Tranceiver is the Device Under Test (DUT) and is commanded to change speed from 10 Mbps to 100 Mbps in either forced or auto-negotiation mode.

1. Read Register 0 (user defined).
2. Put the port into internal 100 Mbps loopback (Register 0 = 0x6100).
3. Read Register 21 to clear.
4. Wait for link up by polling Register bit 17.10 = 1.
5. Send one packet.
6. Read Register 21 again. If it is non-zero, reset the port (Register bit 0.15 = 1).
7. Reprogram the port settings (user defined).
8. Set the port to the desired mode (user defined).

Part B: Use the following sequence if the link partner changes speed from 10 Mbps to 100 Mbps and the DUT has auto-negotiation enabled:

1. When link-down is detected in 10 Mbps mode, read Register 21.
2. If Register 21 is not 0, reset the port by writing Register bit 0.15 = 1.

Workaround 2: If checking for 100 Mbps false errors before resetting a port is not desired, as defined in Workaround 1, Parts A and B, every time speed changes from 10 Mbps and link-down is detected, reset the port by writing Register bit 0.15 = 1.

Status Fixed

Erratum 10: FIFO Lockup

Problem When the LXT9785/LXT9785E PHY Tranceiver is in a link-up state and the receive media is presented with noise that occasionally resembles a Start-of-Stream Delimiter (SSD) symbol, the device may receive the noise and fill the receive FIFO, causing the FIFO to lock up. Example sources of this type of noise could be fiber modules with floating inputs or twisted-pair systems powering up or down.

Implication No packets are sent to the MAC when the FIFO is locked up.

Workaround Managed System:

1. Monitor Register bit 17.6 for FIFO error (Register bit 17.6 = 1).
2. If a FIFO error occurs, reset the locked port (Register 0 = 0x8000).

Status Fixed

Erratum 11: LED Stretch

Problem If all of the following conditions are present, the “transmit” or “receive” LED turns off:

- Full-duplex mode is enabled.
- Any of the three port LEDs are set to indicate transmit or receive activity (Register bits 20.15:12 = 0111).
- LED pulse stretching is enabled (Register bit 20.1 = 1).
- Transmitted and received packets are simultaneously processed through a port.

Note: Normally, the transmit or receive LED is on during activity.

Implication The LED remains off when there is simultaneous transmit and receive traffic.

Workaround Turn off the LED pulse stretching by setting Register bit 20.1 = 0.

Status Fixed

Erratum 12: Far-End Fault Reporting

Problem If a link partner continuously sends successive Far-End Fault (FEF) codes (three sets of 84 1s followed by a 0), the LXT9785/LXT9785E PHY Tranceiver sets the Remote Fault bit High (Register bit 1.4 = 1) and drops link (Register bit 1.2 = 0). Register 1.4 is cleared after a Read and is not set High again while the Far-End Fault signal is present.

Implication If the MAC reads Register bit 1.4 more than once under a continuous Far-End Fault condition, a Far-End Fault is not indicated after the first Read.

Workaround Once a remote fault has been indicated by Register bit 1.4 = 1, the following sequence can be used to monitor the remote-fault status.

Managed Systems:

1. Write Register 0 = 0x6100. This forces the port to 100 Mbps full-duplex internal loopback, link is up, Register 1.2 = 1, and Register 1.4 = 0.
2. Wait approximately 100 mS.
3. Write Register 0 = 0x2100. This forces the port into 100 Mbps full-duplex. If Far-End Fault is present, Register 1.4 = 1 indicates Far-End Fault and Register 1.2 = 0 indicates link is down.

Status Fixed

Erratum 13: Destination Address in 10 Mbps Mode

Problem When the LXT9785/LXT9785E PHY Tranceiver is operating in 10 Mbps mode and preamble byte alignment is enabled (Register bit 18.13 = 1), the LXT9785/LXT9785E PHY Tranceiver drops the second incoming nibble following a 5D if the second nibble following the 5D is a 5 (1010). Subsequent 5s will also be dropped until a non 5 is received.

Note: The MAC will transmit the Least Significant Bit (LSB) first on the byte boundary. For example: A "1 5" will be transmitted as 1010 1000.

Implication Packets received with Destination Addresses starting with '5' will be forwarded to the MAC and dropped.

Some vendors incorrectly hard code the unassigned IEEE MAC address starting with '5' into their products. The following web site lists some of these vendors:

<http://www.cavebear.com/CaveBear/Ethernet/>

Workaround None.

Status Fixed

Erratum 14: Changing Advertised Duplex While Link Is Up

Problem Writing to Register bits 4.9:5, which control duplex mode advertisement while link is up and auto-negotiation is enabled, immediately changes the PHY mode of operation to the new duplex mode. When written, the values in this register are not intended to affect PHY operation until a new auto-negotiation cycle is completed.

Implication A possible mixed-duplex operation will exist during the time between Register bits 4.9:5 writes and the start of a new auto-negotiation process.

Workaround Write Register bits 4.9:5 immediately before the start of a new auto-negotiation process.

Status Fixed

Erratum 15: FIFO Error Bit During FIFO Overwrites

Problem The FIFO Error bit (Register bit 17.6) is not set in the case of FIFO overflows due to large differences between the clock emptying the FIFO and the recovered clock filling the FIFO. One or more packets may be concatenated together, forming one very long corrupted packet.

Implication The concatenated packets will not be detected as a FIFO error. The problem occurs under the following conditions:

- The maximum FIFO setting (Register bits 18.14:15 = 11).
- The maximum system frequency differences (>200 ppm) between the local system clock and the link partner recovered clock.
- When receiving larger (jumbo frames) than standard 1518-byte frames.

Workaround Use MAC layer protocol to capture these errors.

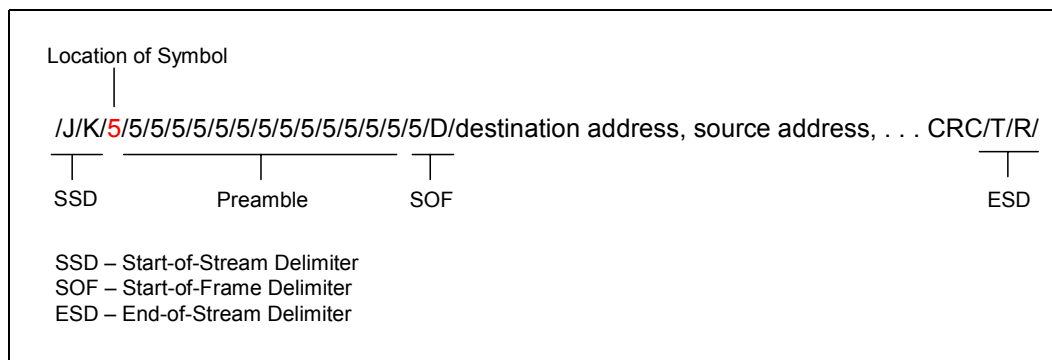
Status No Fix

Erratum 16: SLP Detection in Forced 100 Mbps Mode

- Problem** The Standard Link Partner Detected (SLP_Det) bit (Register bit 27.3) fails to assert when DTE discovery is enabled and the link partner is configured for forced 100 Mbps.
- Implication** If using SLP_Det in the decision to apply power, power may be applied to a standard link partner that does not require in-line power.
- Workaround** Use the Power_En bit (Register bit 27.4) in the decision to apply power.
- Status** No Fix

Erratum 17: Detection of Illegal Symbols After SSD

- Problem** An illegal symbol placed immediately after the SSD (preamble after JK) is not detected. However, any subsequent corrupt symbol will be detected. Below is the standard frame contents:



- Implication** RXER will not assert if this symbol location is corrupted. However, an error in this location does not affect packet integrity.
- Workaround** Use the MAC layer protocol to detect corrupt symbols in the packet.
- Status** No Fix

Erratum 18: RXD[1:0] Signal in RMI I Mode

- Problem** When carrier activity is detected during the initial reception of a packet, CRS_DV is required to be driven active and the pattern "00" is required to be driven on the RXD[1:0] signals until preamble is available from the FIFO. In 100 Mbps mode, the RXD[1:0] signal lines continue to drive Out-of-Band (OOB) signal values for approximately one nibble (40 ns) after CRS_DV goes active, instead of the "00" pattern. After this initial delay, RXD[1:0] drives the expected "00" pattern.
- Implication** The RXD[1:0] signaling anomaly, occurring approximately one nibble after carrier activity is detected, is not expected to cause any data errors. Typically, MAC devices do not look for errors in the data stream until after the Start-of-Frame Delimiter has been detected.
- Workaround** Do not enable OOB signaling (Register 25).
- Status** No Fix



Erratum 19: RMII During False Carrier Event

Problem During a false carrier event, the RMII interface is required to drive “10” on the data interface during the entire carrier event. However, after an initial pattern of “10”, periodic patterns of “11”, “00”, and “01” are driven on the data interface. The RXER signal is Low while the patterns are being driven.

Implication The MAC may not detect false carrier events properly. Runts or short packets may be detected during a false carrier event.

Workaround None.

Status No Fix

Erratum 20: Receive Error Count Register Incrementing

Problem The Receive Error Count Register (Register 21) may not increment, or may increment twice, if the first packet after link is up is an errored packet.

Implication Register 21 may be off by one count.

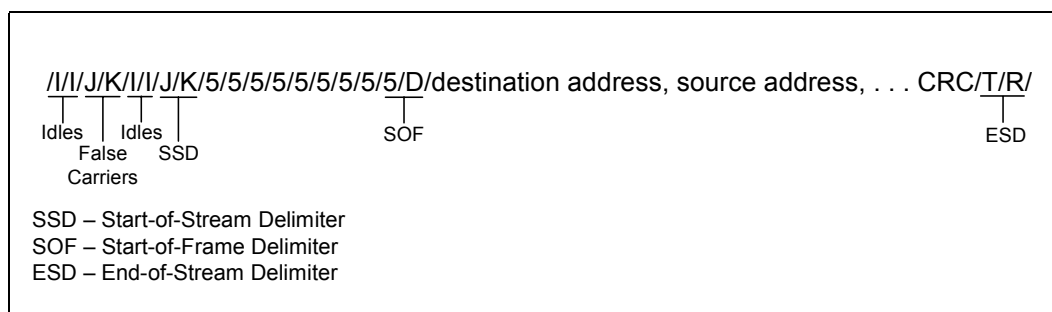
Workaround Read register 21 to clear the value after the first packet is received. Receive error counts will be accurate after the Read.

Status No Fix

Erratum 21: False Carrier Over-Extension

Problem A false carrier event, followed by two idle symbols and a packet, may extend the false carrier event to include the packet in 100 Mbps operation. This false carrier sequence is shown in the false carrier diagram below.

Implication A packet may be seen as a false carrier event and may be dropped. Minimal impact is expected. False carriers occur only when a large number of errors occur due to poor link quality. Below is a diagram of a false carrier:



Workaround None.

Status No Fix

Erratum 22: Power-On-Reset (POR) Configuration Function

- Problem** The hardware configuration pin values are not read during power-up reset when the hardware reset pin is floating or connected to VCC.
- The hardware configuration pins CFG[3:1], FIFO_SEL[1:0], G_FX/TP, MDIX, PAUSE, and PREASEL are not read and captured automatically during power-on reset. These pins are read only by a hardware reset.
- Implication** The PHY device will not be configured as expected by the affected hardware configurations pins.
- Workaround** Hold the hardware reset pin Low until valid voltage supply thresholds are achieved to ensure the proper hardware configuration pin values are read.
- Status** Fixed

Erratum 23: Duplex Status and LED Behavior During DTE Discovery

- Problem** The Duplex LED and the Quick Status Duplex Register bit 17.9 indicate full-duplex status under the following conditions:
- Auto-negotiation with DTE Discovery is enabled (and) (Register bits 0.12 and 27.6 are set)
 - An IP phone has been detected by the LXT9785/LXT9785E PHY Transceiver (and) (Register bit 27.4 is set)
 - 100BASE-TX Duplex bit is enabled (and) (Register bit 4.8 is set)
 - Duplex LED is enabled (Register bits 20.15:12 or 20.11:8 or 20.7:4 are set to '0101' or '1110')
- The Duplex Quick Status bit (Register bit 4.8) and the Duplex LED indicate full-duplex status from the time a DTE device (IP Phone) is detected (Register bit 27.4 is set) until one of the following occurs:
- Auto-negotiation is restarted
 - A forced speed/duplex mode is enabled
 - Register bit 4.8 is cleared
- Implication** During the time period defined above, full-duplex status may be indicated to the system software by Register bit 17.9 and indicated on the Duplex LED.
- Workaround** The following may be used when an IP Phone is detected (Register bit 27.4 is set):
- Immediately clear Register bit 4.8 if it is set.
 - No action is necessary if Register bit 4.8 is not set.
- Status** No Fix

6.0 Specification Changes

There are no specification changes.

7.0 Specification Clarifications

Item 1: LXT9785/LXT9785E PHY Transceiver Operating Conditions Table

Description The modified version of Table 1 will be replaced in the next revision of the LXT9785/LXT9785E Datasheet. Changes are shown in bold/italic and the cells are highlighted.

Table 8 LXT9785/LXT9785E PHY Transceiver Operating Conditions

Parameter		Sym	Min	Typ ¹ (2.5 V _{ccio})	Typ ¹ (3.3 V _{ccio})	Max	Units
Commercial Operating Temperature	Ambient	T _{op} a	0	–	–	70	°C
	Case	T _{op} c	25	–	–	108	°C
Extended Operating Temperature	Ambient	T _{op} a	-40			85	°C
	Case	T _{op} c	-15			123	°C
1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing. 2. Voltages with respect to ground unless otherwise specified. 3. Values are aggregated for all eight ports.							

8.0 Documentation Changes

Item 1: BGA15 Twisted-Pair Signal Description Update

Description Table notes 2 and 3 were omitted from Table 39, LXT9785/LXT9785E PHY Transceiver Signal Descriptions of the LXT9785/LXT9785E Datasheet.

Add the following notes #2 and #3 to Table 39, LXT9785/LXT9785E PHY Transceiver Signal Descriptions of the LXT9785/LXT9785E Datasheet.

Note #2: Switched to Inputs (see TPIP/N description) when MDIX is not active [that is, twisted-pair, non-crossover MDI mode].

Note #3: Switched to Outputs (see TPOP/N description) when MDIX is not active [that is, twisted-pair, non-crossover MDI mode].

Documents LXT9785/LXT9785E Datasheet

Status Fixed. This change has been made in the LXT9785/LXT9785E Datasheet, Revision 11.0.

Item 2: Cable Diagnostic Behavior In Forced 10BASE-T Mode

Description Up to 100 bits (10 μ s) of 100BASE-TX, MLT3 idle symbols are transmitted when exiting Cable Diagnostic mode (clearing Register bit 29.10) in forced 10BASE-T mode. As a workaround, Use Cable Diagnostics in forced 100BASE-TX mode only. This item has no known system effect.

The LXT9785/LXT9785E Datasheet will be updated to indicate that the forced 100BASE-TX mode should be used for Cable Diagnostics tests to avoid this behavior.

Documents LXT9785/LXT9785E Datasheet

Status Fixed. This change has been made in the LXT9785/LXT9785E Datasheet, Revision 11.0.



For additional product and ordering information:

www.cortina-systems.com