Cortina Systems® LXT9785/9785E Design and Layout Guide

Application Note

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*Other names and brands may be claimed as the property of others.

Contents

Figures

Tables

Revision History

Revision 4.0 Revision Date: 14 March 2007
First release of this document from Cortina Systems, Inc.

Revision 003 Revision Date: 04 December 4 2002
Replaced text under Section 6.2, “Fiber Interface”.
Modified Figure 17, “Recommended LXT9785/9785E-to-3.3V Fiber Transceiver Interface Circuitry”.
Modified Figure 18, “Recommended LXT9785/9785E-to-5V Fiber Transceiver Interface Circuitry”.

Revision 002 Revision Date: January 2002
Globally replaced LXT9785 with LXT9785/9785E.
Replaced Section 6.2. with new text.
Replaced Figure 17.
Added Figure 18.
Added Figure 19.

Revision 001 Revision Date: February 2001
System Clock Requirements: Modify language for clock requirements.
Twisted-Pair Interface Circuitry: Add table note 3.
Bob Smith Termination: Change to NIC setup.
Magnetics Manufacturers: Change TransPower part number from “SH2P1” to “RJS08-766P1-C”.
Fiber Interface diagram: Change 2D_2P5V to SD_2P5V.

1.0 General Description

This application note provides detailed design and layout guidelines to achieve optimum performance in high-density systems using Cortina Systems® LXT9785/9785E 8-Port 10⁄100 Mbps Transceiver PHY (LXT9785⁄9785E PHY) products. Adherence to these guidelines helps to ensure a successful design that meets IEEE requirements.

The following topics are discussed in this document:

Design Guidelines: Good design practices prevent most common signal and noise issues. General guidelines listed in this section should be followed throughout the entire design.

Power and Ground: This section covers layout of the power and ground planes and internal routing of power and ground signals. Also included are some tips to avoid creating loop antenna effect.

MII Interfaces: The Reduced Media Independent Interface (RMII), Serial Media Independent Interface (SMII), and Source Synchronous Serial Media Independent Interface (SS-SMII) are discussed in this section.

Network Interfaces: Termination circuitry for the twisted-pair interface is provided in this section. Ideal biasing networks that attach to an external fiber optic transceiver are also shown for the fiber interface.

Magnetic Requirements: This section details the magnetic specifications. Before committing to a specific component, designers should contact the manufacturer for current product specifications and validate components for each application.

The LXT9785⁄9785E PHY is an 8-port Fast Ethernet PHY Transceiver that supports IEEE 802.3 physical layer applications at both 10 Mbps and 100 Mbps Mbps. It provides all three Serial/ Source Synchronous and Reduced Media Independent Interfaces (SMII/SS-SMII and RMII) for switching and other independent port applications.

2.0 General Design Guidelines

2.1 Introduction

Meeting EMI and ESD requirements and achieving maximum line performance depends on good design practices. These practices minimize high-speed digital switching noise and common-mode noise, and provide shielding between internal circuits and the environment. Good design practices apply *throughout* the entire design, not just to the LXT9785⁄9785E PHY, and include the following:

2.2 General Recommendations

- Verify all components meet application requirements. Use component listings only for reference.
- Follow the guidelines for designing and laying out the twisted-pair and/or fiber interfaces, including standard practices for differential signals and guidelines for optimizing return loss performance.
- Provide termination on all high-speed switching signals and clock lines.
- Provide impedance matching on long traces to prevent reflections.

2.3 Power and Ground Filtering

- Follow good design practices to minimize noise from digital switching and power supply circuits.
- Ensure the power supply is rated for the load.
- Keep power and ground noise levels below 50 mV.
- Filter the analog power circuits. The filters may be removed if performance testing proves they are unnecessary.
- Filter and shield DC-DC converters, oscillators, etc.

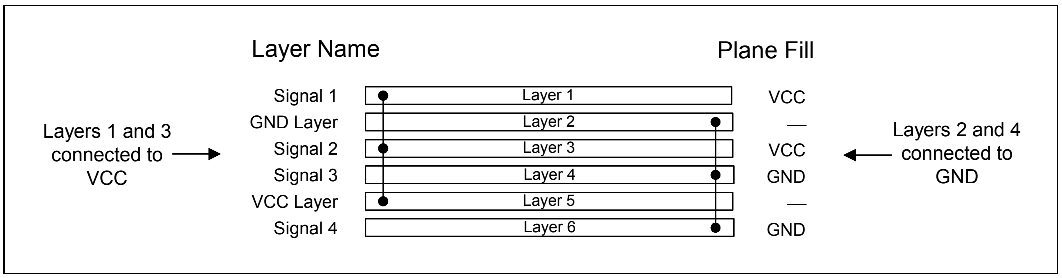
2.4 Decoupling and Bulk Caps

- Use bulk capacitors (4.7-10 μF) between the power and ground planes to minimize power-supply switching noise.
- Use an ample supply of .01 μF decoupling capacitors to reduce high-frequency noise on the power and ground planes.

2.5 Power and Ground Planes

- Provide ample power and ground planes.
- Avoid breaks in the ground plane, especially in areas where it is shielding high-frequency signals.
- Route high-speed signals adjacent to a continuous, unbroken ground plane.
- When possible, fill in unused areas of the signal planes with solid copper and attach them with vias to a VCC or ground plane that is not located adjacent to the signal layer. This technique (see Figure 1) is referred to as signal layer filling and can improve capacitive coupling of the power planes.
- Stagger vias to avoid creating moats in the planes caused by anti-pad voids.

Figure 1 Signal Layer Filling



2.6 Magnetic "Safe Zone"

- Void power and ground planes directly under the magnetics. Use chassis ground in the area from the magnetics to the RJ-45 connector.
- Keep high-speed signals out of the area between the LXT9785⁄9785E PHY and the magnetics.
- Do not route any digital signals between the LXT9785⁄9785E PHY and the RJ-45 connectors at the edge of the board.

2.7 Differential Signal Layout

- Route differential pairs close together and away from other signals.
- Keep both traces of each differential pair as identical to each other as possible.
- Keep each differential pair on the same plane.
- Minimize vias and layer changes.
- Keep transmit and receive pairs away from each other; run orthogonally, or separate with a ground plane layer.

2.8 Boundary Scan Interface

The LXT9785⁄9785E PHY device supports an IEEE 1149.1 Boundary Scan Test Interface for board level testing. This interface consists of five pins (TMS, TDI, TDO, TRST, and TCK). Boundary Scan Input pins have internal termination and may be left floating when not in use.

2.9 System Clock Requirements

The LXT9785⁄9785E PHY requires a 50 MHz, +\- 50 ppm reference clock when configured for RMII mode. The reference clock (REFCLK) must be enabled at all times. Characteristics of the 50 MHz clock include:

- Duty cycle distortion no greater than 40 to 60%.
- Voltage levels: VOH > 2.0 V for VCCIO = 3.3 V +/- 5%; VOH > 1.75 V for VCCIO = 2.5 V +/- 5%.

The LXT9785⁄9785E PHY requires a 125 MHz, +\- 50 ppm ppm reference clock when configured for either SMII or SS-SMII modes. The reference clock (REFCLK) must be enabled at all times. Characteristics of the 125 MHz clock include:

- Duty cycle distortion no greater than 40 to 60%.
- Voltage levels: VOH > 2.0 V for VCCIO = 3.3 V +/- 5%; VOH > 1.75 V for VCCIO = 2.5 V +/- 5%.

The reference clock is used to generate transmit signals and recover receive signals. A crystal-based clock is recommended over a derived clock (i.e., PLL-based) to minimize transmit jitter. Regardless of clock source, careful consideration should be given to physical placement, board layout, and signal routing of the source to maintain the highest possible level of signal integrity. See the Clock Layout Guidelines below for more details and refer to Table 1 on page 8 for a list of recommended oscillators.

For applications that use a single 8-port sectionalization, RefClk0 and RefClk1 must always be tied together and to the source.

2.9.1 Clock Layout Guidelines

- Keep the clock traces as short as possible.
- Route the clock traces adjacent to an unbroken ground plane.
- Use a multi-output clock driver when driving multiple inputs with a single oscillator.
- Individually terminate point-to-point interconnects to every clock load. Series termination is the most common termination technique.

Table 1 Oscillator Manufacturers

Manufacturer	Part Number	Frequency
CTS	MXO45 / 45LV	50 MHz
Saronix	ST4130A	125 MHz

3.0 Power and Ground Design

3.1 Power and Ground Planes

For high-speed communications design, the power and ground planes may be conceptually divided into four regions (the analog and digital power planes and the chassis and signal ground planes) as shown in Figure 1 on page 7.

3.1.1 Power Planes

The LXT9785⁄9785E PHY is a 2.5 V device. The analog supplies (VCCR and VCCT) as well as the core digital supply (VCCD) require 2.5 V +\- 5%. The digital I/O supply supports either a 2.5 V or 3.3 V supply to facilitate interfacing 2.5 V or 3.3 V controllers.

3.1.1.1 Analog VCC Plane

The analog power region extends from the magnetics back to the LXT9785⁄9785E PHY. The power plane in this area should be filtered. Only components and signals pertaining to the analog interface should be placed or routed through this region. The analog plane supplies power to the VCCR and VCCT pins of the LXT9785⁄9785E PHY as shown in Figure 3 on page 10.

3.1.1.2 Digital VCC Plane

The digital power region extends from the MII interfaces of the LXT9785⁄9785E PHY through the rest of the board. Follow good design practices listed in the previous section throughout this area. The digital plane supplies power to VCCD and VCCIO as shown in Figure 2 on page 10. External components such as oscillators and MACs should also be supplied from the digital plane.

3.1.2 Ground Planes

3.1.2.1 Signal Ground

The signal ground region should be one continuous, unbroken plane extending from the magnetics through the rest of the board. GNDD, GNDA, and GNDS should be directly connected to the signal ground plane.

Signal ground planes often have high-frequency noise caused by returning signal currents. While these high-frequency fluctuations are too small to cause issues in the digital circuits, they are large enough to exceed FCC limits and are often coupled onto signals running outside the digital block. The use of magnetics and chassis ground is a common solution to minimize high-frequency noise emissions from the logic ground plane.

3.1.2.2 Chassis Ground

A chassis ground plane can be added to the layer stack. Place this plane directly next to a ground plane to create a very tight capacitive coupling between the two planes. The chassis plane should then be multi-point connected to the external chassis.

Chassis ground can also be combined with the signal ground layer. For isolation, place a “moat” around the signal ground plane to separate signal ground from chassis ground.

The chassis ground region extends from the front edge of the board (RJ-45 connectors) to the magnetics, and around the perimeter of the board. No signals should pass through this region except for external interfaces and LED signals.

3.1.3 Avoiding Loop Antenna Effects

When laying out ground planes, take special care to avoid creating loop antenna effect.

- Run all ground planes as solid square or rectangular regions.
- Avoid creating loops with ground planes around other planes. The only exception to this rule is chassis ground as shown in Figure 2.
- Ensure the chassis ground loop (running the perimeter of the board) is voided at some point.
- Ensure the gap of the voided area in chassis ground is large enough to prevent a ground loop.

Figure 2 Power and Ground Placement

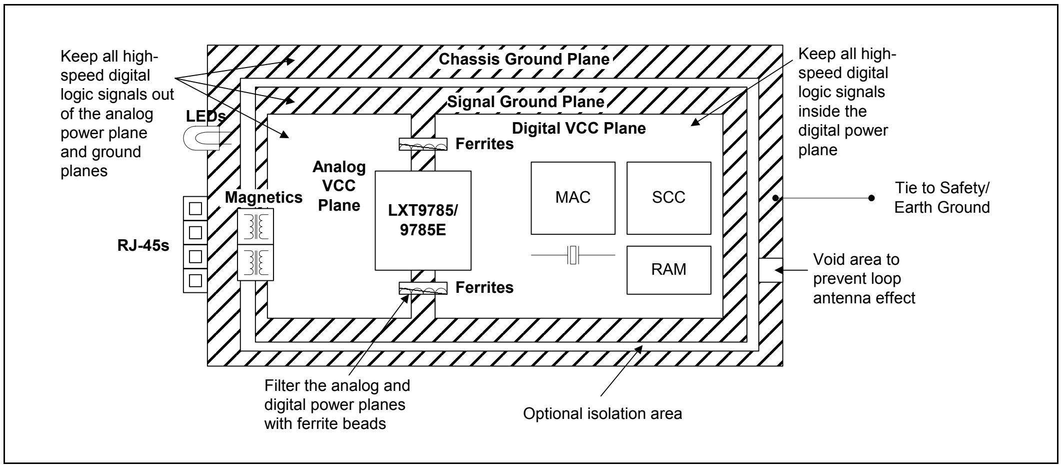
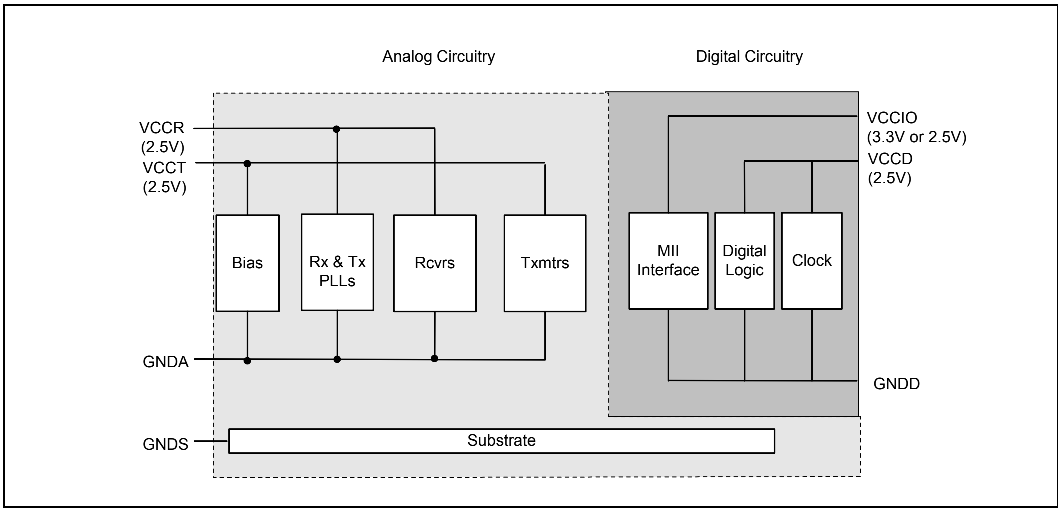


Figure 3 Internal Routing of Analog and Digital Power Signals



3.2 Design Considerations

Power supply ripple and digital switching noise can be created by:

- Poorly-regulated or over-burdened power supplies.
- Data busses running at high clock rates.
- DC-to-DC converters.

Noise created by these sources can be coupled into the transmitter and receiver and out onto the network. Coupling may also occur through the LXT9785⁄9785E PHY analog power and ground pins or other termination circuits such as magnetic center taps. See the Network Interfaces section on page 24. This condition contributes to EMI and data corruption.

Use the criteria found in Table 2 for evaluating acceptable noise levels in the analog region of the power and ground planes.

Table 2 Criteria for Analog Noise Levels

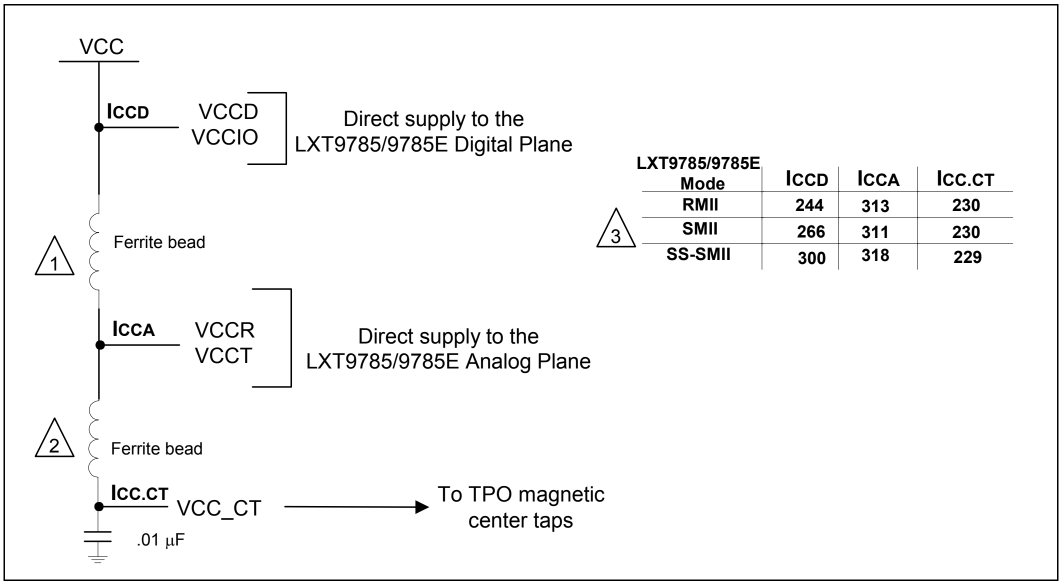
Noise Level	Acceptability
Under 50 mV	Acceptable
50 mV to 80 mV	Marginally Acceptable
Above 80 mV	Unacceptable

3.3 Design Implementation

Following good general design and layout guidelines prevents most common signal and noise issues. The following recommendations apply to the design and layout of the power and ground planes:

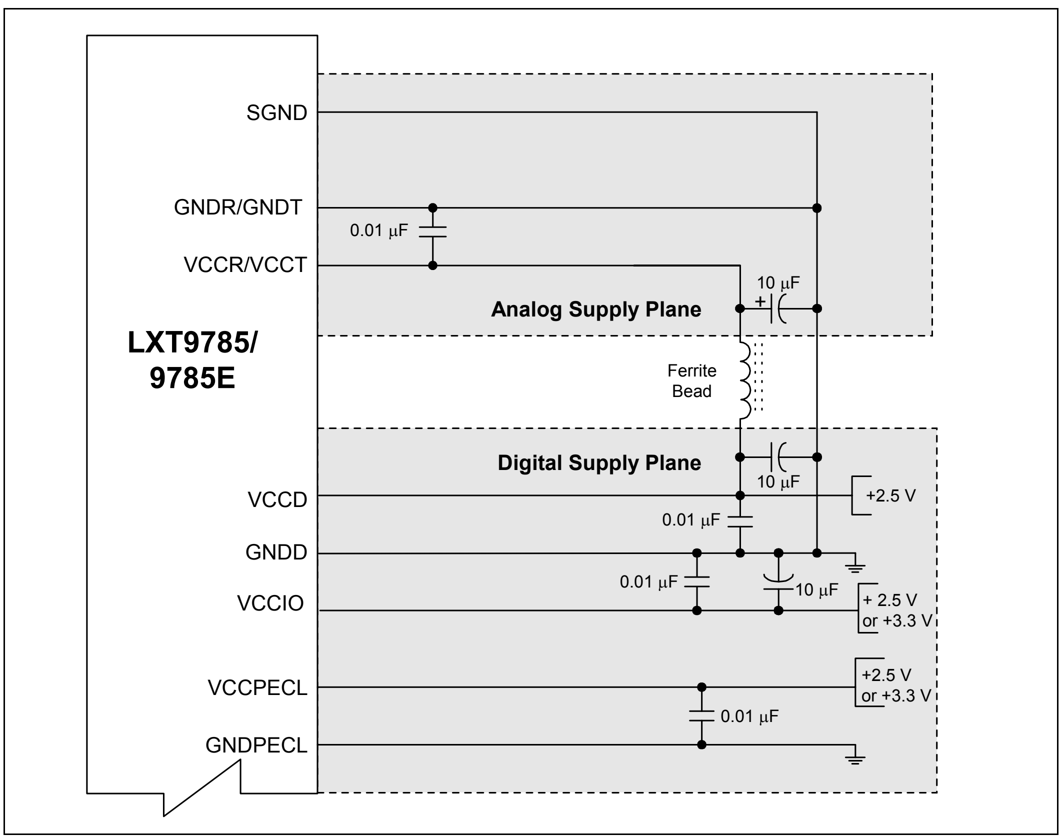
- Divide the VCC plane into two sections (analog and digital) as shown in Figure 2 on page 10. The break between the two planes should run under the device.
- When dividing the VCC plane, it is not necessary to add extra layers to the board. Simply create moats or cut-out regions in existing layers.
- Join the digital and analog sections at one or more points by ferrite beads. Ensure the maximum current rating of each bead is at least 150% of the nominal current that is expected to flow through it. See Figure 4 for current load listings.
- Place a bulk capacitor (10 µF) on each side of each ferrite bead to stop switching noise from traveling through the ferrite.
- For designs with multiple LXT9785⁄9785E PHYs, it is acceptable to supply all from one analog VCC plane. This plane can be joined to the digital VCC plane at multiple points, with a ferrite bead at each point. It is also acceptable to create an individual analog VCC *mini-plane* for each device.
- To improve EMI performance, use a ferrite bead between the analog voltage plane and the magnetic transmit center tap as shown in Figure 4. A single bead per port should be used for optimum benefit.
- Place a high-frequency bypass cap (.01 µF) near each VCC pin as shown in Figure 5 on page 12.
- Place a 10 µF bulk capacitor close to the device between VCCIO and GNDD.
- Use a continuous, unbroken ground plane.

Figure 4 Power Supply Current



LXT9785/9785E Mode	ICCD	ICCA	ICC.CT
RMII	244	313	230
SMII	266	311	230
SS-SMII	300	318	229

Figure 5 Power and Ground Decoupling



4.0 MII Interfaces

4.1 Optimized MIIs

The LXT9785⁄9785E PHY may be configured to support either the Reduced Media Independent Interface (RMII), Serial Media Independent Interface (SMII), or Source Synchronous Serial Media Independent Interface (SS-SMII) via hardware. Table 3 describes the Mode Select configuration requirements for each mode.

Table 3 MII Mode Select Configurations

MII Mode	MODESEL_1 Input	MODESEL_0 Input
RMII	0	0
SMII	0	1
SS-SMII	1	0
Reserved	1	1

These optimized Media Independent interfaces, RMII, SMII, and SS-SMII, reduce the number of pins required for the MAC interface in high-density switch applications. A single external synchronous clock reference simplifies the clock interface.

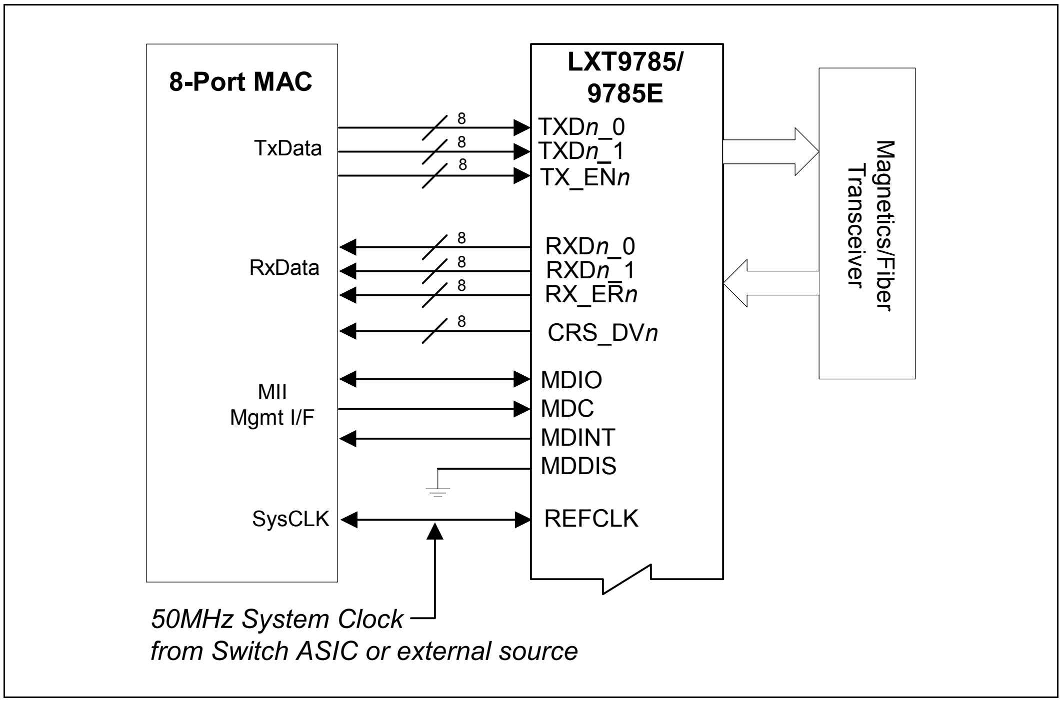
4.1.1 Reduced MII (RMII)

The LXT9785⁄9785E PHYprovides an RMII for each network port. The RMII uses four signals to pass received data to the MAC (RXD*n*<1:0>, RX_ER*n*, and CRS_DV*n*). Three signals are used to transmit data from the MAC (TXD*n*<1:0> and TX_EN*n*). This interface operates at 50 MHz and requires a single 50 MHz reference clock for both the receive and transmit signals.

The RMII data interface for the LXT9785⁄9785E PHY is shown in Figure 6. Data is transmitted across the RMII interface in 2-bit nibblets or di-bits. The LXT9785⁄9785E PHY provides a parallel/serial converter that translates between di-bit pairs and 4-bit nibbles.

The LXT9785⁄9785E PHY RMII has an output impedance of 14Ω and normally only requires termination on the output signals in designs with long traces (>3 inches). Place the resistor as close to the device as possible. Use a software trace termination package to select an optimal resistance value for the specific trace. If this is not possible, use a 50Ω resistance value.

Figure 6 RMII Interface

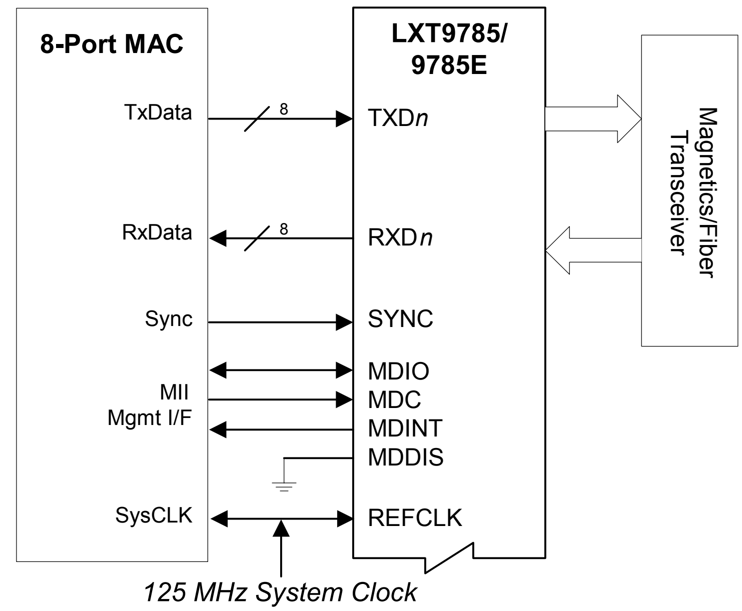


4.1.2 Serial MII (SMII)

The LXT9785⁄9785E PHY provides an SMII for each network port. As shown in Figure 7, the SMII uses one signal to pass received data to the MAC (RXD*n*) and one signal to pass transmit data from the MAC (TXD*n*). The SMII operates at 125 MHz using a global reference clock and frame synchronization signal (REFCLK and SYNC). The SMII data flow is shown in Figure 7. Data is transmitted across the SMII interface in 10-bit serial words. Each word contains one data byte (two nibbles of 4B coded data) and two status bits.

The LXT9785⁄9785E PHY has an output impedance of 11Ω. Use series termination resistors on all output signals to minimize reflections. Select the series resistor value to match the effective trace impedance. If the trace impedance is not known, use a 33Ω resistance value.

Figure 7 SMII Interface

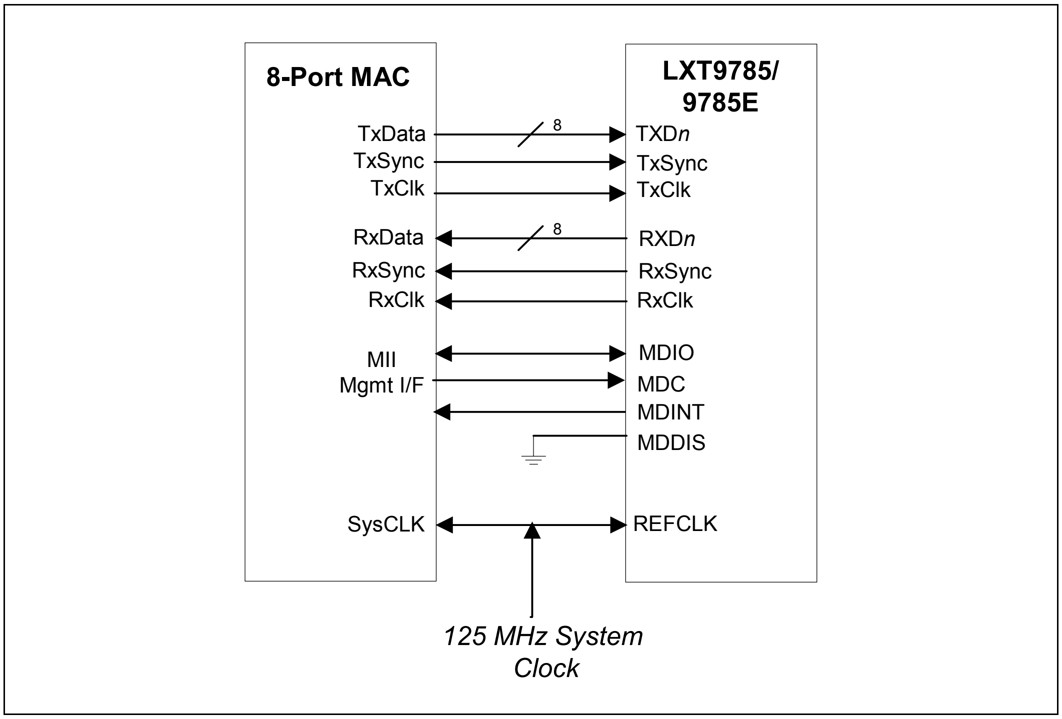


4.1.3 Source Synchronous MII (SS-SMII)

The LXT9785⁄9785E PHY provides an SS-SMII for each network port. As shown in Figure 8, the SS-SMII uses one signal to pass received data to the MAC (RXD*n*) and one signal to pass transmit data from the MAC (TXD*n*). The SS-SMII operates at 125 MHz using independent global transmit and receive reference clock and frame synchronization signals (TX-CLK, TX_SYNC, RX_CLK, and RX_SYNC. The SS-SMII data flow is shown in Figure 8. Data is transmitted across the SS-SMII interface in 10-bit serial words. Each word contains one data byte (two nibbles of 4B coded data) and two status bits.

The LXT9785⁄9785E PHY has an output impedance of 8Ω. Use series termination resistors on all output signals to minimize reflections. Select the series resistance value match of the effective trace impedance. If the trace impedance is now known, use a 33 Ω resistance value.

Figure 8 SS-SMII Interface



5.0 MII Sectionalization

The LXT9785⁄9785E PHY allows increased flexibility when interfacing high-port count MACs and ASICs. The device may be configured via the SECTION pin into a single 8-port device or into two separate 4-port sections, each with its own MII and MDIO interface (see Figure 10, Figure 12, and Figure 14). This sectionalization requires independent control for both sections via duplicate REFCLK, SYNC, MDIO, and MDC signals as shown in Figure 10, Figure 12, and Figure 14.

For all applications that use 8-port sectionalization, RefClk0 and RefClk1 must always be tied together at the source. See Table 4 for Clock/SYNC requirements for RMII, SMII, and SS-SMII modes.

Table 4 Clock/SYNC Requirements for RMII, SMII and SS-SMI Modes

RMII Sectionalization		SMII Sectionalization		SS-SMII Sectionalization	
Mode	Signals	Mode	Signals	Mode	Signals
1x8	Ref_Clk0	1x8	Ref_Clk0	1x8	Ref_Clk0
	Ref_Clk1		Ref_Clk1		Ref_Clk1
			SYNC0		Tx_CLK0
					Tx_SYNC0
					Rx_CLK1
					Rx_SYNC1
2x4	Ref_Clk0	2x4	Ref_Clk0	2x4	Ref_Clk0
	Ref_Clk1		Ref_Clk1		Ref_Clk1
			SYNC1		Tx_CLK0
					Tx_CLK1
					Tx_SYNC0
					Tx_SYNC1
					Rx_CLK0
					Rx_CLK1
					Rx_SYNC0
					Rx_SYNC1

Figure 9 Typical RMII Interface Diagram

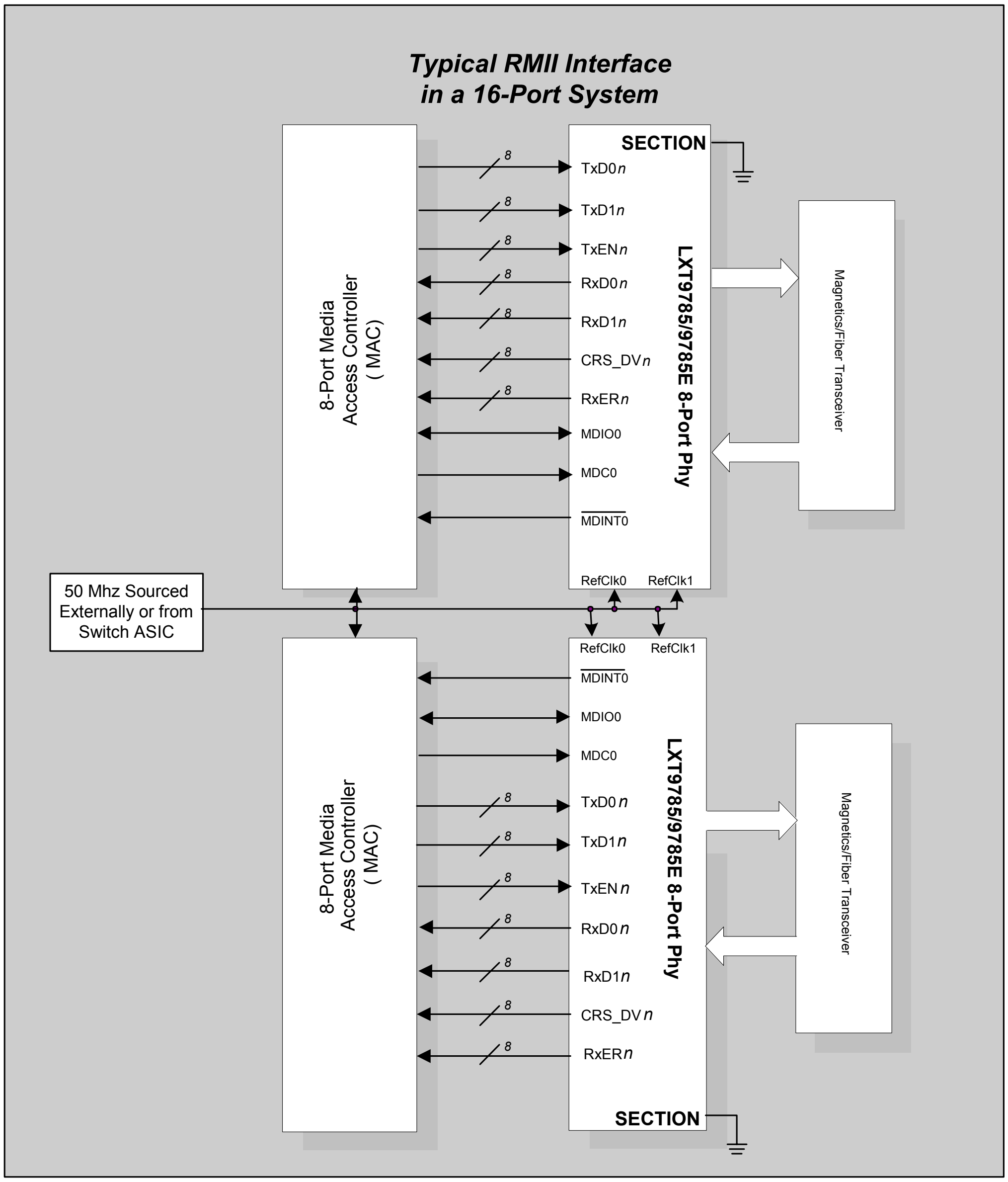


Figure 10 Typical RMII Quad Sectionalization Diagram

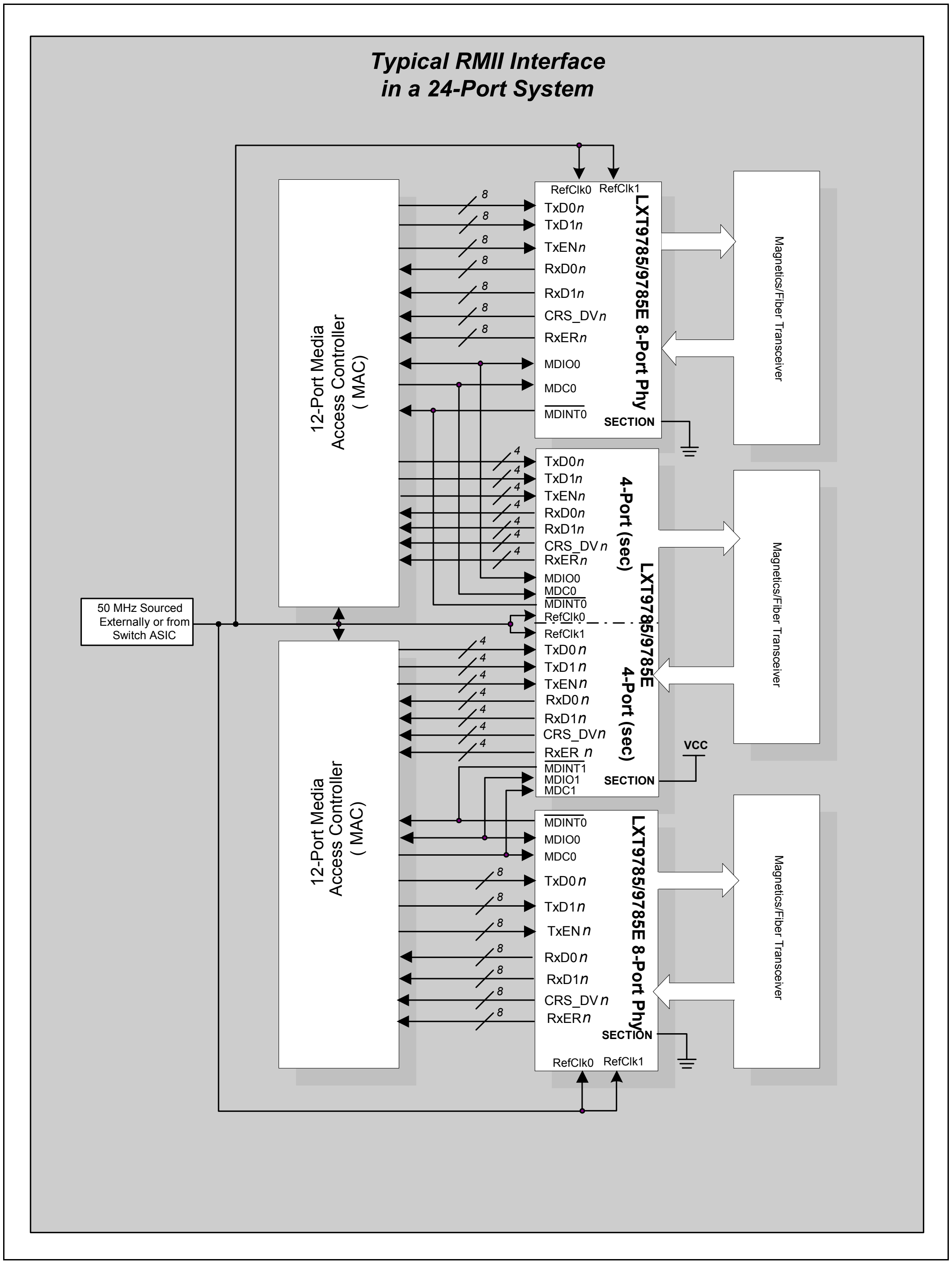


Figure 11 Typical SMII Interface Diagram

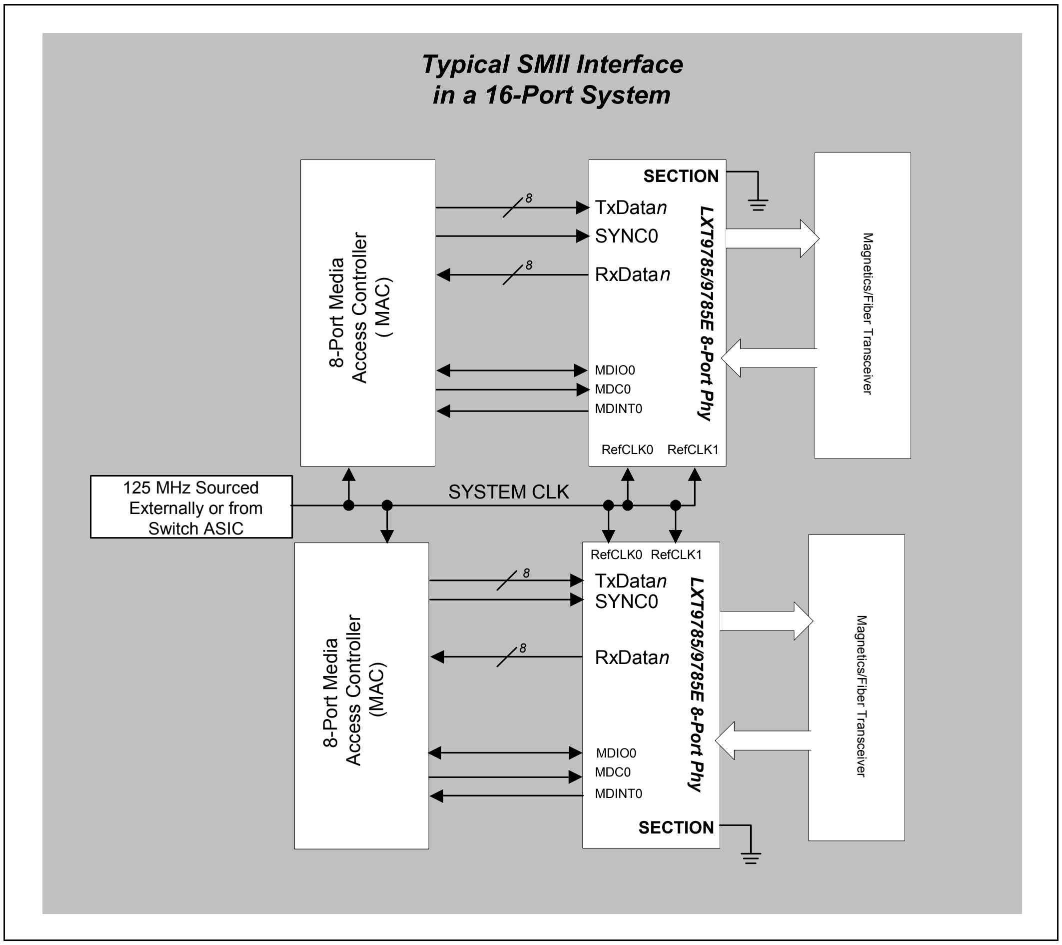


Figure 12 Typical SMII Quad Sectionalization Diagram

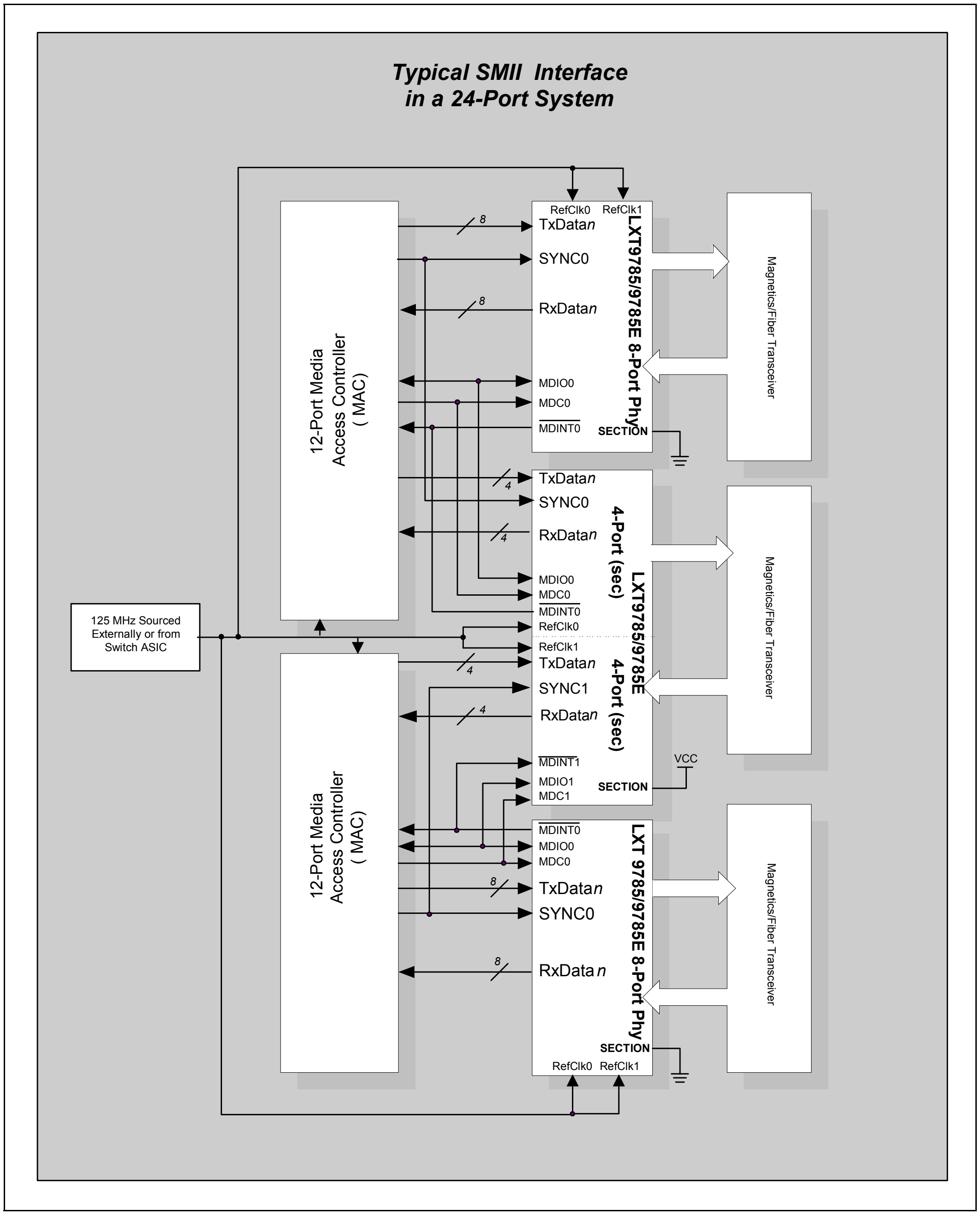


Figure 13 Typical SS-SMII Interface Diagram

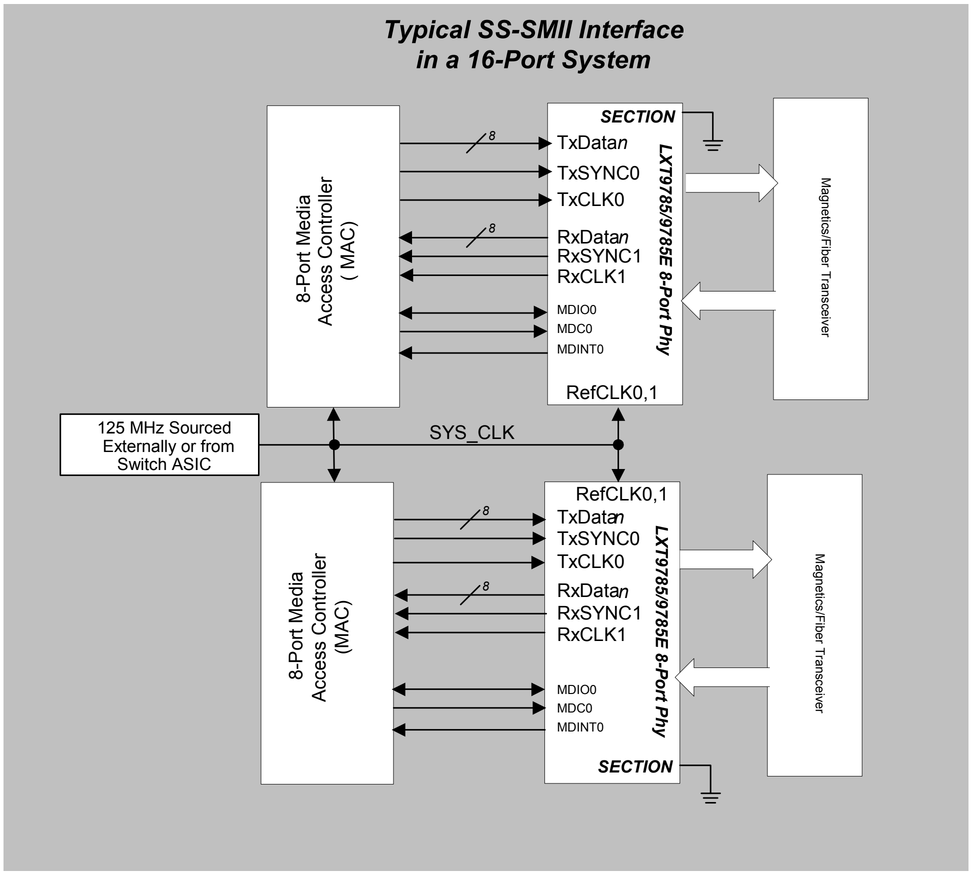
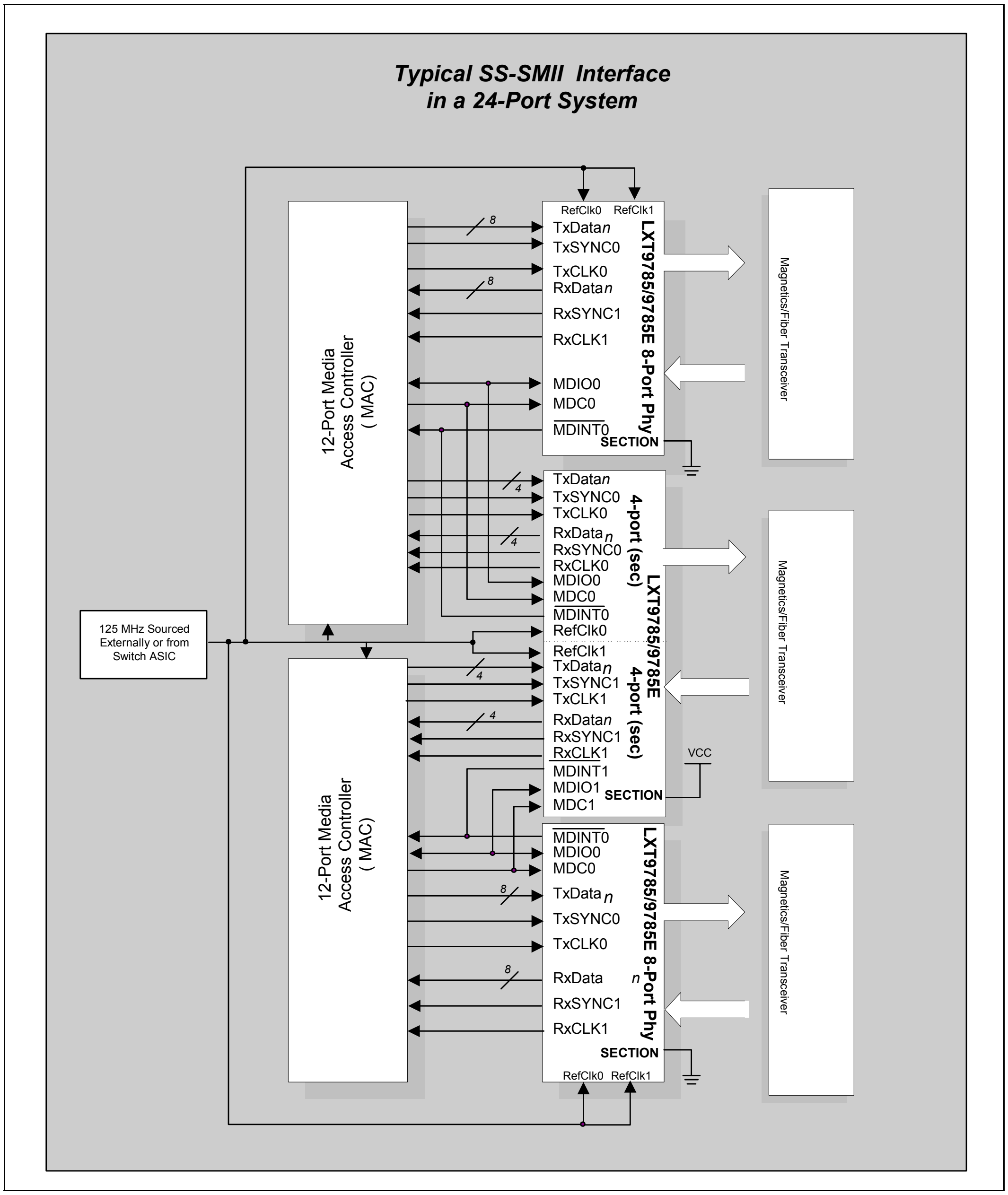


Figure 14 Typical SS-SMII Quad Sectionalization Diagram



6.0 Network Interfaces

6.1 Twisted-Pair Interface

The twisted-pair interface consists of magnetics, connectors, and termination circuitry commonly referred to as Bob Smith Termination.

The recommended interface circuitry with magnetics is shown in Figure 15. This circuit includes:

- Magnetic center tap (device side) tied to VCCT via a ferrite bead and bypassed to GNDA using a 0.01 µF capacitor.
- One ferrite bead per port, rated at 50 mA, to supply center tap current. A single ferrite bead per device rated at 400 mA is also acceptable but may not provide optimal benefit.

Unlike last generation transceivers, the LXT9785⁄9785E PHY does not require any of the external load termination typically required to match the 100 Ω characteristic impedance of an unshielded CAT5 twisted-pair wire. The external resistors that are typically required on both the transmit and receive pairs for impedance matching have been integrated into the LXT9785⁄9785E PHY. The internal termination provides a constant current reference in both 10BASE-T and 100BASE-TX applications and meets all IEEE transmitter requirements, such as return loss, while greatly reducing external component requirements.

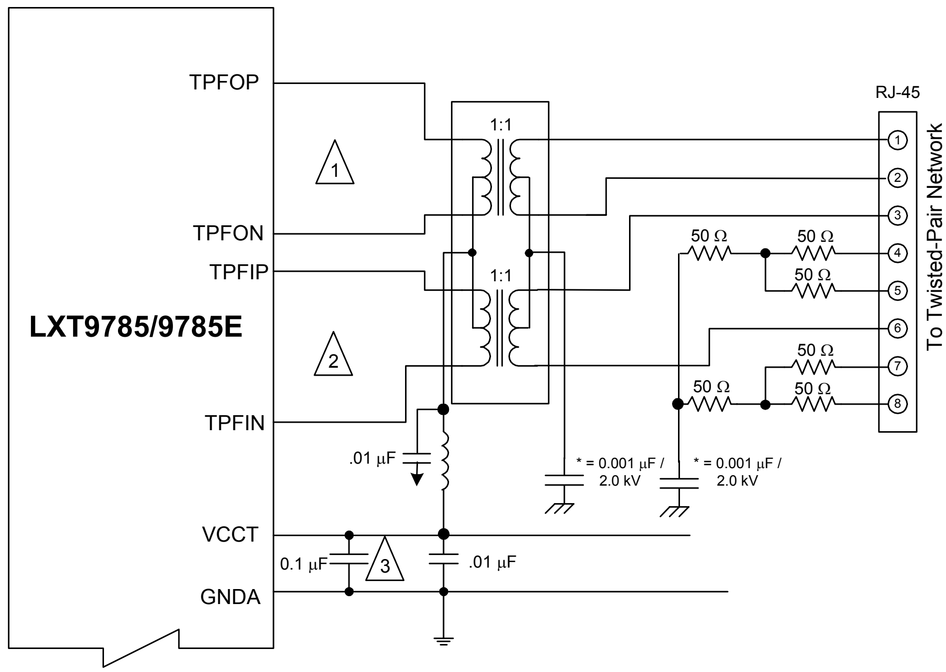
Note: In designs using twisted-pair only, it is recommended that the VCCPECL inputs be connected to ground to save power.

6.1.1 Common Mode Choke

The magnetics typically include a common-mode choke. Some vendors place the choke on the line-side (secondary) of the main winding, while others place it on the device side (primary).

The line-side center tap can be bypassed to chassis ground, but this should be carefully evaluated in the system application. Bypassing both center taps of the transmit winding may produce undesirable results by creating a low impedance AC coupling between the chassis ground and circuit ground. Consider potential noise sources and ground plane characteristics when evaluating bypass options.

Figure 15 Twisted-Pair Interface Circuitry



1. The 100 Ω transmit load termination resistor typically required is integrated in the LXT9785⁄9785E PHY.
2. The 100 Ω receive load termination resistor typically required is integrated in the LXT9785⁄9785E PHY.
3. Recommended 0.1 µF capacitor to improve EMI performance.

6.1.2 Meeting IEEE Requirements

Focus on two key areas to optimize return loss performance with the LXT9785⁄9785E PHY. First, minimize shunt capacitance on the board. Second, carefully select the magnetics.

Adherence to the following guidelines helps to ensure each design meets IEEE requirements for the 100TX PMD layer as called out in the ANSI X3.263 specification.

6.1.3 Guidelines for Reducing System Shunt Capacitance.

- Avoid multiple layer changes in TPFON/P and TPFIN/P signal routing.
- Keep the magnetics as close as possible to the LXT9785⁄9785E PHY, and keep TPFOP and TPFON traces as short as possible.
- Use quad magnetics optimized for dual-high RJ-45 connectors to allow the most compact layout.
- Use the termination circuit shown in Figure 16 on page 26.
- Provide EMI shielding by placing a ground plane under TPFOP, TPFON, and the magnetics.

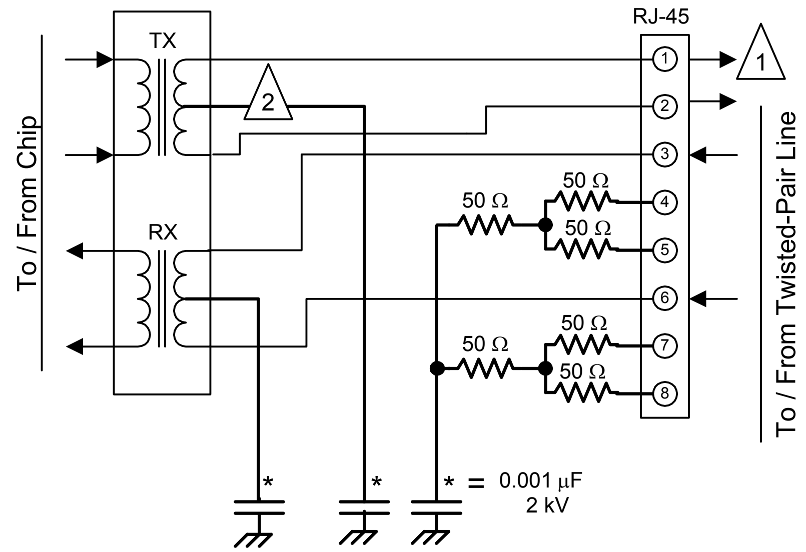
6.1.4 Bob Smith Termination

A “Bob Smith” termination is often provided for the unused signal pairs of the twisted-pair interface (RJ-45 pins 4, 5, 7, and 8) and the media-side center taps. This circuit is used to enhance EMI and ESD performance of the system. Although there are many variations on this technique, one common implementation is shown in Figure 16. Note the signals are referenced to chassis ground rather than circuit ground.

The Bob Smith termination can be broken down into two circuits. One circuit provides termination for the unused signal pairs of the twisted-pair interface. The unused pairs are connected together through a 75 Ω impedance matching circuit, and then to chassis ground through a 0.001 µF, 2 kV capacitor. The capacitor provides a discharge path for noise immunity on the unused pairs.

The second circuit provides termination for the media-side center taps and is comprised of individual 0.001 µF, 2 kV capacitors to chassis ground. Separate capacitors are used for the receive and transmit center taps. This improves isolation by eliminating the low impedance path between receiver and transmitter that would exist if a single common capacitor were used. The capacitors provide a high-frequency path to ground, enhancing ESD and EMI performance.

Figure 16 Bob Smith Termination Circuit



1. RJ-45 connections shown for standard NIC. Tx/Rx crossover may be required for switch applications.
2. Magnetics without a receive pair center tap do not require a 2 kV termination.

6.1.5 Magnetic Requirements

The LXT9785⁄9785E PHY requires a 1:1 ratio for both the receive transformers and the transmit transformers. The transmit isolation voltage should be rated at 1.5 kV to protect the circuitry from static voltages across the connectors and cables. Refer to Table 5 for magnetic requirements.

In order to support the Auto-MDIX functionality of the LXT9785⁄9785E PHY, the magnetic must provide a center tap for both the transmit and receive magnetic winding. VCCT must be connected to both as shown in Figure 15 on page 25.

Table 6 provides a list of magnetic manufacturers and part numbers. This list constitutes a reference only and is not a recommendation. It is the responsibility of the system designer to ensure that all components, both individually and collectively, are suitable for the intended application.

Table 5 Magnetic Requirements

Parameter	Min	Nom	Max	Units	Test Condition
Rx turns ratio	–	1 : 1	–	–	–
Tx turns ratio	–	1 : 1	–	–	–
Insertion loss	0.0	0.6	1.1	dB	–
Primary inductance	350	–	–	µH	–
Transformer isolation	–	1.5	–	kV	–
Differential to common mode rejection	40	–	–	dB	.1 to 60 MHz
	35	–	–	dB	60 to 100 MHz
Return Loss	-16	–	–	dB	30 MHz
	-10	–	–	dB	80 MHz

Table 6 Magnetic Manufacturers

Product	Port/Ratio	Manufacturer[1]	Part Numbers Quad-Port	
LXT9785/9785E	Rx = 1:1 Tx = 1:1	Bel Fuse	S558-5999-Q9	(Quad)
		Delta	LF8731	(Quad)
		Halo	TG110-AMX2NX	(Quad)
		InNet	T0465S	(Quad)
		Midcom	7144-37	(Quad)
		Pulse	H1164	(Quad)
			J2042H3A	Integrated Magnetics
		TransPower	RJS08-766P1-C	Integrated Magnetic

1. Device manufacturers may have additional magnetics with varying pinouts.

6.2 Fiber Interface

The fiber interface consists of two Low-Voltage Positive Emitter Coupled Logic (LVPECL) signal pairs that attach to an external fiber optic transceiver. Both 3.3 V fiber optic transceivers (see Figure 17) and 5 V fiber optic transceivers (see Figure 18 and Figure 19) can be used with the LXT9785⁄9785E PHY. See the 100BASE-FX Fiber Optic Transceivers-Connecting a PECL/LVPECL Interface Application Note (document number 250781) for detailed information on fiber interface designs and recommendations for Cortina PHYs.

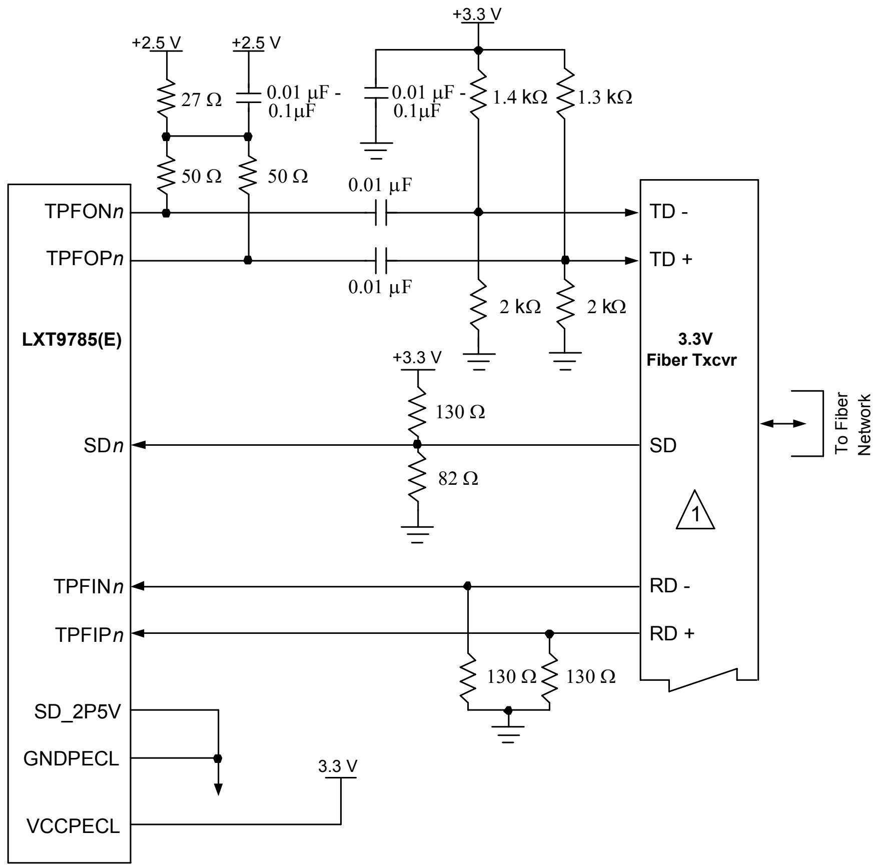
The following should occur in 3.3 V fiber transceiver applications as shown in Figure 17:

- The transmit pair should be AC-coupled with 2.5 V supplies (the circuitry on the LXT9785⁄9785E PHY side of the capacitors is used to set the proper differential voltage from the LXT9785⁄9785E PHY current sources) and re-biased to 3.3 V LVPECL levels.
- The transmit pair should contain a 1.3 kΩ -1.4 kΩ balance offset to prevent PHY-to-fiber transceiver crosstalk amplification in power-down, loopback, and reset states (see the fiber interface application note).
- The receive pair should be DC-coupled to the fiber transceiver with a 130 Ω emitter current path.
- The signal detect pin should be DC-coupled with a 50 Ω single-ended emitter current path to 1.3 V.

The following should occur in 5 V fiber transceiver applications as shown in Figure 18:

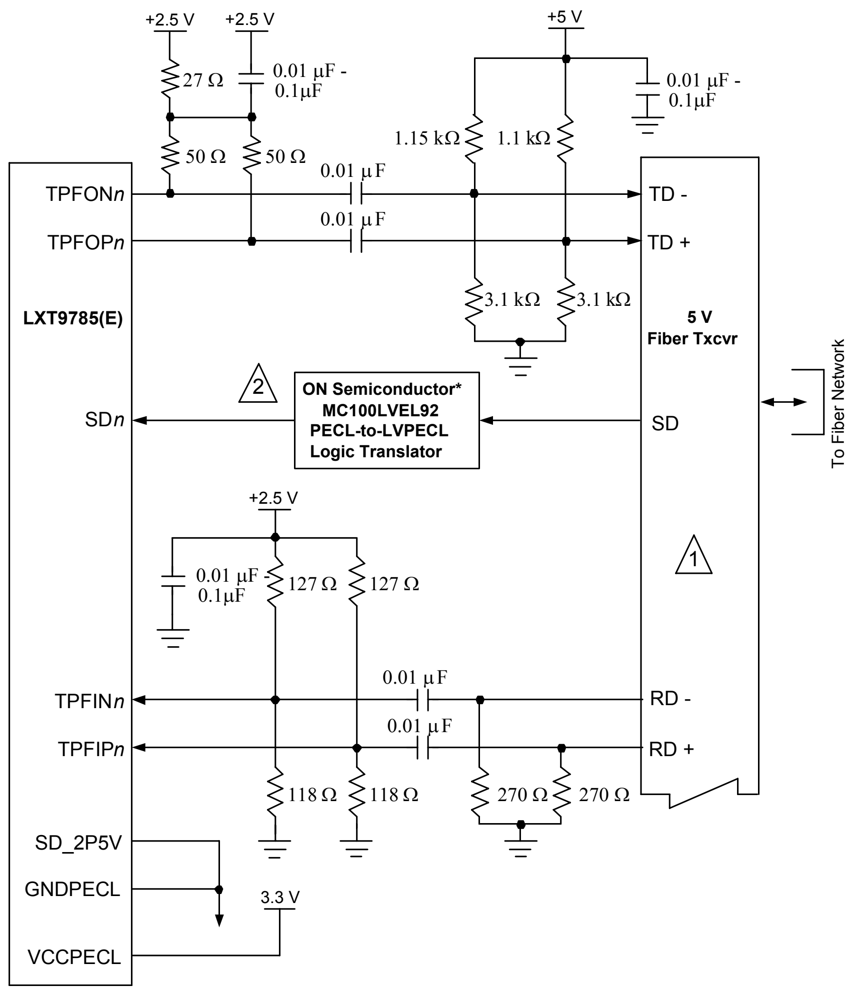
- The transmit pair is always AC-coupled, and re-biased to 3.7 V on the fiber transceiver side of the capacitors (the circuitry on the LXT9785⁄9785E PHY side of the capacitors is used to set the proper differential voltage from the LXT9785⁄9785E PHY current sources).
- The transmit pair should contain a 1.1 kΩ-1.15 kΩ balance offset to prevent PHY-to-fiber transceiver crosstalk amplification in power-down, loopback, and reset states (see fiber interface application note).
- The receive pair is always AC-coupled, and re-biased to 1.2 V on the LXT9785⁄9785E PHY side (the 270 Ω pull-down resistors provide an emitter current path for the fiber transceiver outputs).
- The signal detect pin should use a PECL-to-LVPECL logic translator as shown in Figure 19.

Figure 17 Recommended LXT9785⁄9785E PHY-to-3.3V Fiber Transceiver Interface Circuitry



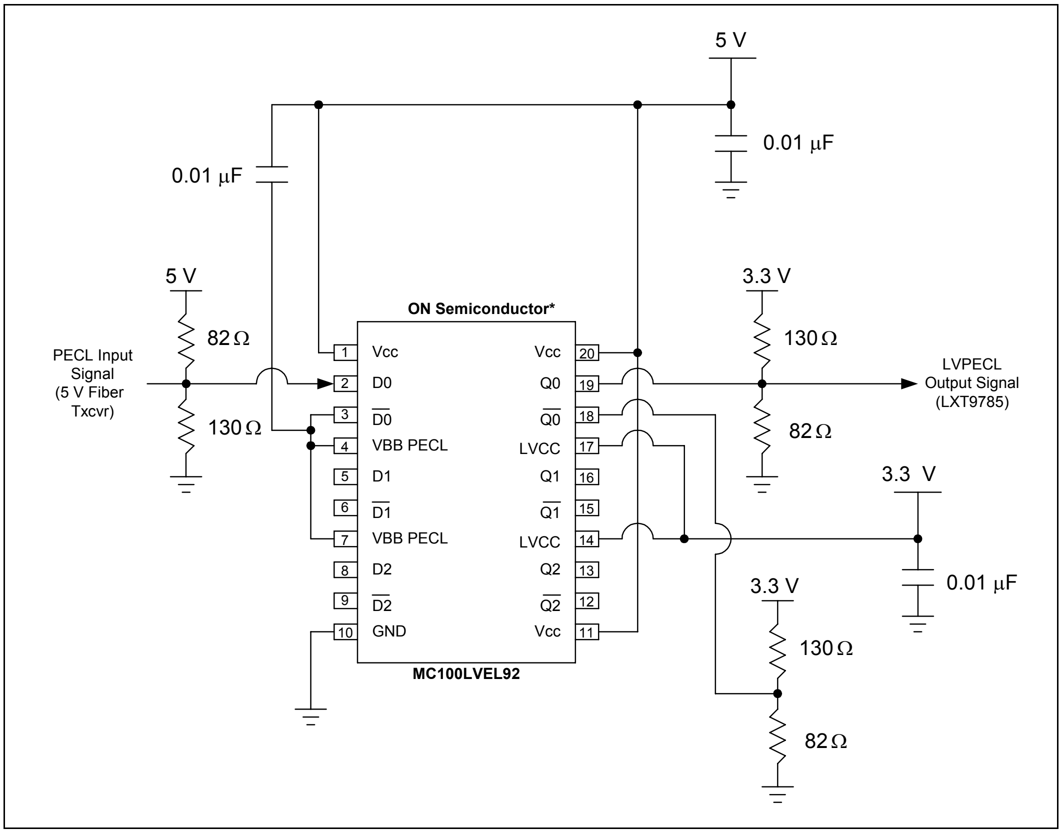
1. Refer to the transceiver manufacturers' recommendations for termination circuitry.

Figure 18 Recommended LXT9785⁄9785E PHY-to-5V Fiber Transceiver Interface Circuitry



1. Refer to the transceiver manufacturers' recommendations for termination circuitry.
2. See Figure 19 on page 31 for recommended logic translator interface circuitry.

Figure 19 ON Semiconductor Triple PECL-to-LVPECL Translator



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