Migrating from the Cortina Systems® LXT9784 to the Cortina Systems® LXT9785/LXT9785E

Application Note

26 September 2007

Document Number 250678

Revision 3.0

Contents

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Revision History

Revision 3.0 Revision Date: 26 September 2007
First release of this document from Cortina Systems, Inc.

Revision 002 Revision Date: 03 December 2002
• Modified Table 1, *Twisted-Pair/Fiber Interface Comparison*, on page 7– changed “Pseudo ECL (PECL)” to “Low-Voltage PECL (LVPECL). • Replaced Figure 2, *Network Fiber Interface Circuit for the LXT9785/LXT9785E Transceiver*, on page 9. • Removed Section 3.2, *Signal Comparison of Twisted-Pair and Fiber Modes*.

Revision 001 Revision Date: 01 November 2002
Initial release

1.0 Introduction

Cortina Systems® LXT9785/LXT9785E and LXT9784 8-port Fast Ethernet 10/100 Transceivers support IEEE 802.3 physical layer applications. Both devices provide a Reduced Media Independent Interface (RMII) and a Serial Media Independent Interface (SMII). All network ports provide a twisted-pair (TP) interface for a 10BASE-T/ 100BASE-TX connection.

Although the LXT9785/9785E and LXT9784 Transceivers are similar in many respects, the LXT9785/LXT9785E Transceiver incorporates several functional enhancements for a more robust Ethernet solution, including the following:

- Source Synchronous/Serial Media Independent Interface (SS-SMII) for serial switching and other independent port applications.
- Combination twisted-pair or fiber interfaces for both 10 Mbps and 100 Mbps.

1.1 About this Document

The LXT9784 Transceiver is classified by Cortina Systems, Inc. (Cortina) as “not recommended for new designs.” Although the device remains available for existing designs, new designs using this device are not recommended and may not be supported. The purpose of this document, therefore, is to provide customers with guidelines for migrating existing LXT9784 Transceiver designs, or LXT9784 Transceiver-based designs that may be currently in development, to the more robust and feature-enhanced LXT9785/ LXT9785E Transceiver.

This document has been designed to discuss the differences between the devices in an effort to support and ease design migration concerns and questions. It is not a step-by-step migration planner, as each application may require unique changes to software or other design components that must be addressed by customers individually. As outlined in this document, the LXT9785/LXT9785E Transceiver can provide feature enhancements when compared to the LXT9784 Transceiver.

Section 2.0, *Document Overview*, on page 6 provides the sections and subsections that discuss and illustrate the differences between the LXT9784 Transceiver and LXT9785/ LXT9785E Transceiver devices.

2.0 Document Overview

2.1 Feature Comparison

Comparisons of the LXT9784 Transceiver and LXT9785/LXT9785E Transceiver feature sets are grouped into Analog, Digital, and General categories.

2.1.1 Analog Interface

Section 3.0, *Analog Interface* contains the following sections:

- Section 3.1, *Twisted-Pair and Fiber Interfaces*, on page 7 illustrates the differences in the twisted-pair and fiber interfaces of the devices with tables and diagrams.
- Section 3.2, *RBIAS*, on page 10 describes the differences in the RBIAS setup.

2.1.2 Digital Interface

Section 4.0, *Digital Interface*, on page 11 illustrates and discusses the differences in the digital interface of the LXT9784 Transceiver and LXT9785/LXT9785E Transceiver. It contains the following sections:

- Section 4.1, *Sectionalization*, on page 11 provides a discussion and diagrams of the Sectionalization feature of the LXT9785/LXT9785E Transceiver. This feature is not supported by the LXT9784 Transceiver.
- Section 4.2, *Mode Controls and Indicators*, on page 15 describes mode controls and indicators with manual/hardware controls and MDIO/software controls.
- Section 4.3, *Hardware Configuration Settings*, on page 16 provides the hardware configuration settings for the LXT9785/LXT9785E Transceiver and LED functionality of the LXT9784 Transceiver.
- Section 4.4, *RMII, SMII, and SS-SMII Interfaces*, on page 17 gives a comparison of the MII, RMII, SMII, and SS-SMII interfaces.
- Section 4.5, *Register Sets*, on page 18 lists the register sets for the devices and desribes the Register bit comparisons.
- Section 4.6, *LED Drivers*, on page 18 describes the device LEDs and provides the configuration status bits for the LXT9785/LXT9785E Transceiver.

2.1.3 General

Section 5.0, *General*, on page 19 discusses device differences. It contains the following sections:

- Section 5.1, *Power Management*, on page 19 describes power supply, support for lower voltage MACS, power-down modes, and transmit driver supply.
- Section 5.2, *JTAG Boundary Scan*, on page 20 contains information on JTAG and boundary scan.
- Section 5.3, *Package and Temperature Options*, on page 20 provides packaging and temperature options.
- Section 5.4, *Ball Assignments*, on page 20 provides a listing of the pin assignments for the LXT9784 Transceiver and LXT9785/LXT9785E Transceiver.

3.0 Analog Interface

3.1 Twisted-Pair and Fiber Interfaces

The LXT9784 Transceiver and LXT9785/LXT9785E Transceiver have many of the same functions but display some differences in twisted-pair and fiber interfaces. Table 1 provides a comparison.

Table 1 Twisted-Pair/Fiber Interface Comparison

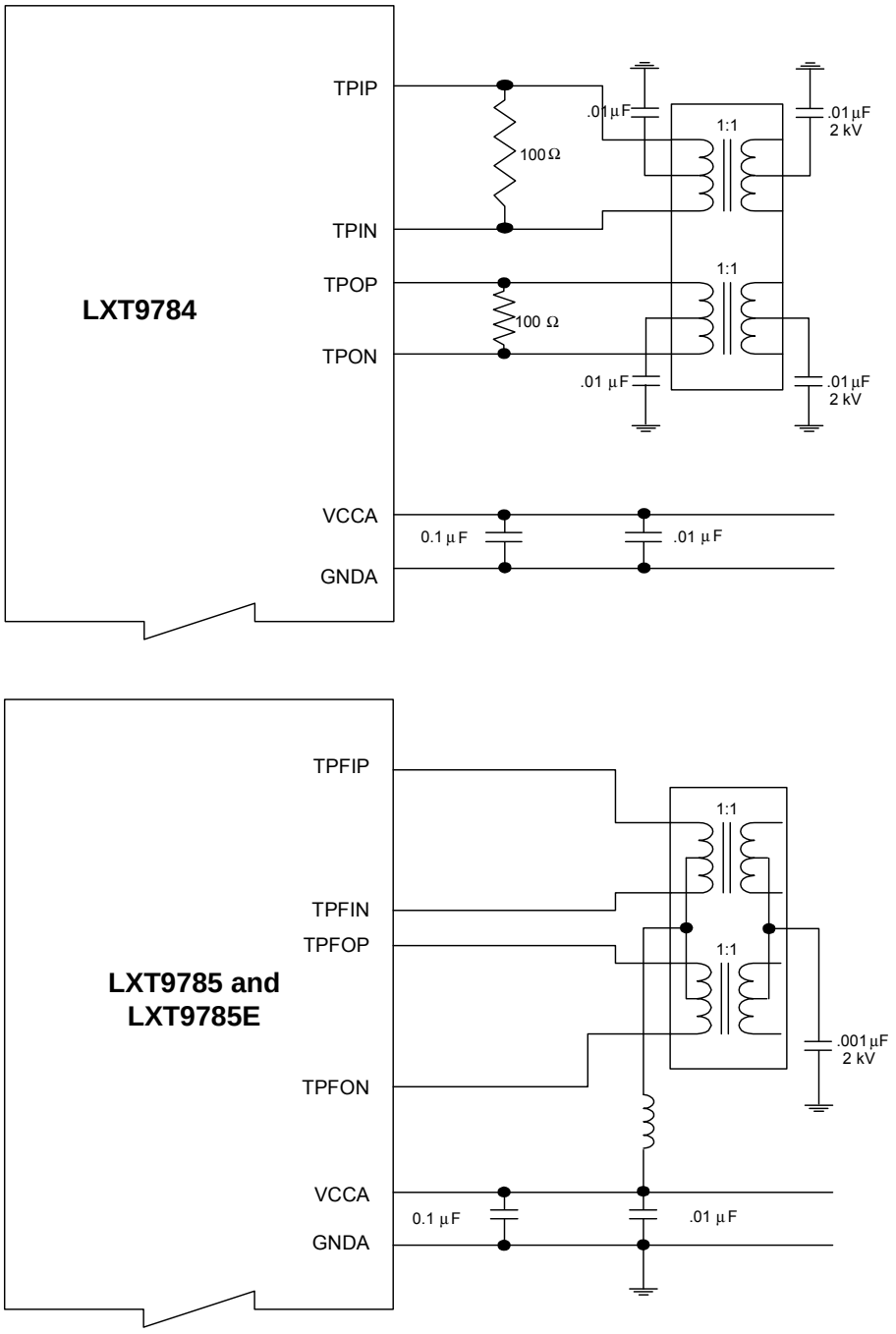
Function	LXT9784 Transceiver	LXT9785/LXT9785E Transceiver
	Signal Description	Signal Description
Twisted-Pair Interface	Supports a twisted-pair network via a single set of pins. See Figure 1 on page 8 and Figure 2 on page 9 for external circuitry comparisons.	Same
Transmit Source	Uses voltage driven output stages. There is no need for an external voltage to drive the device signals.	Uses current driven output stages. The device needs an external center-tap voltage to drive its signals.
	Supports auto MDI/MDIX.	Same
Transmit and Receive Termination Circuitry	Requires external 100Ω load-balancing resistors on the twisted-pair output.	Termination resistors are integrated.
Fiber Interface	Not supported	Supports twisted-pair and fiber networks via a single set of pins. Fiber applications are supported via a Low-Voltage Positive Emitter Coupled Logic (LVPECL) interface to external fiber modules. All ports are selected for twisted-pair or fiber when configured via hardware, and can only be intermixed via software using Register bit 16.0.
Hardware Integrity	Available for each port via Register 29.	Not supported.

Table 2 provides a network interface comparison for the LXT9784 Transceiver and LXT9785/LXT9785E Transceiver and Figure 1 on page 8 and Figure 2 on page 9 provide network interface circuit comparisons for the devices.

Table 2 Network Line Interface Comparison

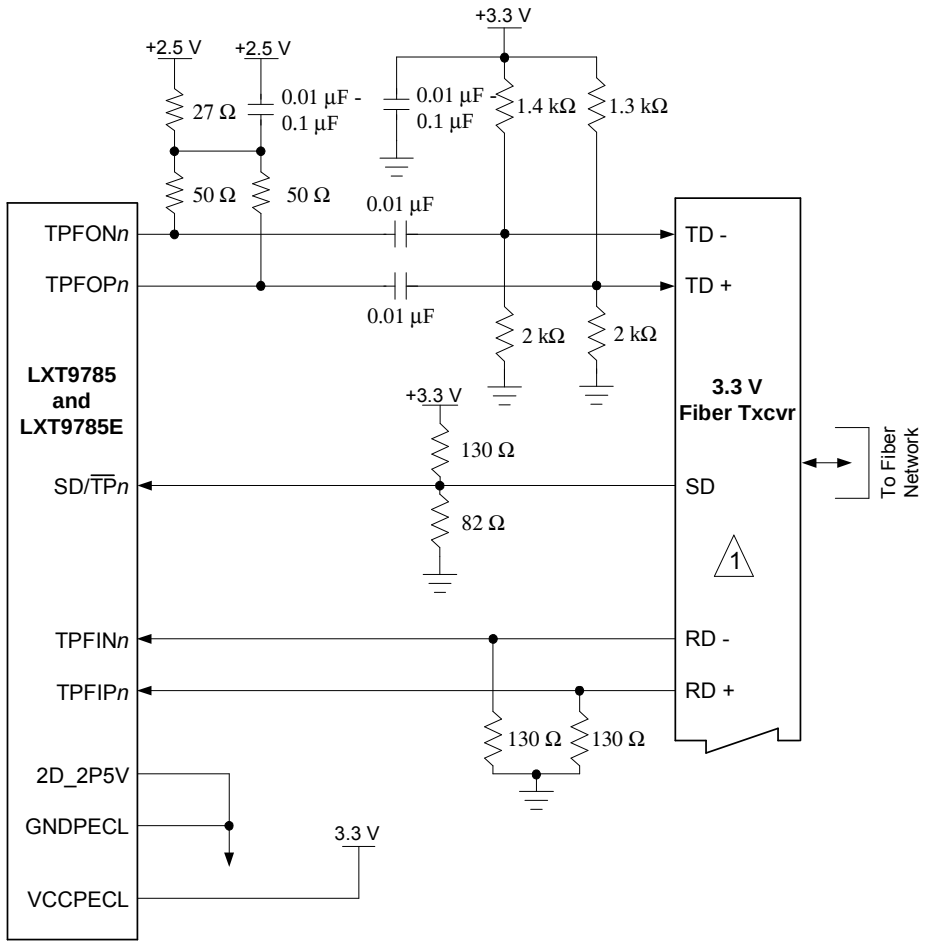
Feature	LXT9784 Transceiver	LXT9785/LXT9785E Transceiver
Auto MDI/MDIX	Auto MDI/MDIX automatically detects the link partner's transmitting cable pair, effectively allowing the connection of either a crossover cable or a patch cable to the device without additional external logic. Auto MDI/MDIX can be selected or disabled via Register bit 28.7. There is no hardware selection pin for auto MDI/MDIX.	Auto MDI/MDIX automatically detects the link partner's transmitting cable pair, effectively allowing the connection of either a crossover cable or a patch cable to the device without additional external logic. Auto MDI/MDIX may be disabled via Register bits 27.9:8 for each port, or by using the hardware configuration pins to enable/disable all eight ports.

Figure 1 Network Twisted-Pair Interface Circuit Comparison



1. Both devices require a 1:1 ratio transformer for the transmit and receive twisted-pairs. The center taps in the LXT9785/LXT9785E Transceiver magnetics are connected together, while the center taps in the LXT9784 Transceiver are not connected.

Figure 2 Network Fiber Interface Circuit for the LXT9785/LXT9785E Transceiver



1. Refer to the transceiver manufacturers' recommendations for termination circuitry.

Note: The LXT9784 Transceiver does not support fiber applications.

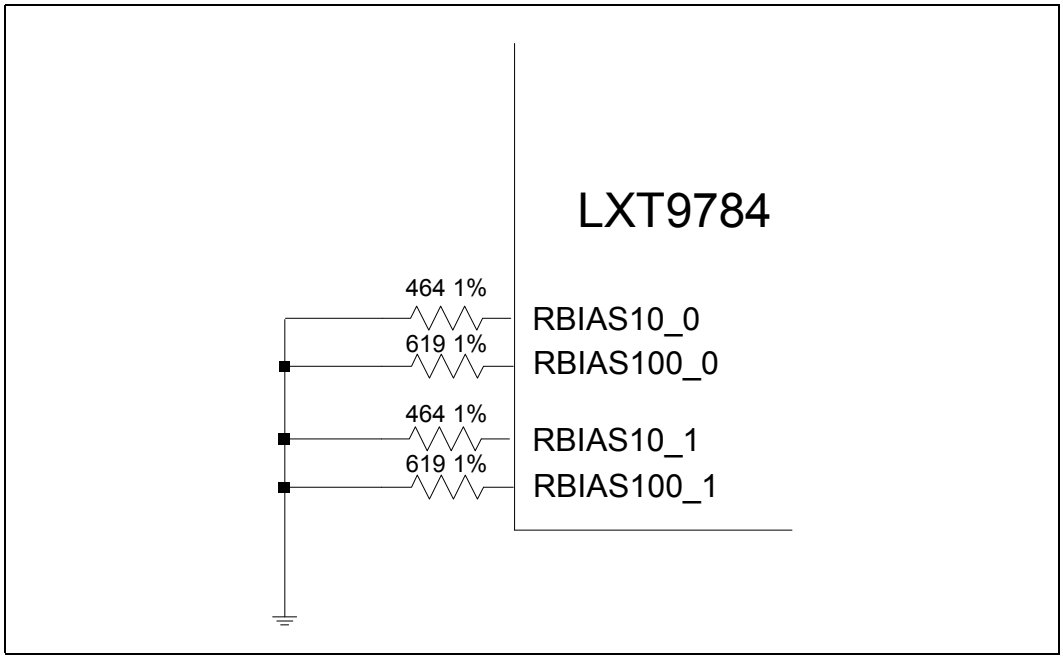
3.2 RBIAS

The LXT9784 Transceiver requires two RBIAS pins for 10 Mbps and 100 Mbps. The RBIAS pin in the LXT9784 Transceiver provides bias current for internal circuitry that must be tied to ground through the following:

- A 464 Ω 1 % resistor for RBIAS10_0 and RBIAS10_1
- A 619 Ω 1 % resistor for RBIAS100_0 and RBIAS100_1.

Figure 3 illustrates a typical RBIAS circuit in the LXT9784 Transceiver. The RBIAS resistor is integrated in the LXT9785/LXT9785E Transceiver.

Figure 3 Typical RBIAS Circuit for LXT9784 Transceiver



4.0 Digital Interface

4.1 Sectionalization

The LXT9785/LXT9785E Transceiver support a Sectionalization feature that is not supported by the LXT9784 Transceiver. This feature allows the chip to be sectionalized into two quad sections, splitting the MDIO bus into two separate PHY access ports. Ports 0-3 of the MDIO section operate independently of ports 4-7. The MII isolate function is unaffected and operates normally.

Sectionalization is selected by pulling Section pin 176 High on the initial power-up sequence as seen in Figure 4. In applications needing Sectionalization such as 2x4 (two quad sections) that have a single MDIO bus structure, the addressing scheme must be contiguous. For example, the first eight ports are addressed with the base Address at 0 (0-7), so the next four ports must be addressed with the base Address at 8 (8-11). See Figure 5 on page 13 and Figure 6 on page 14 for the SMII and SS-SMII Sectionalization diagrams.

Figure 4 LXT9785/LXT9785E Transceiver RMII Quad Sectionalization Diagram

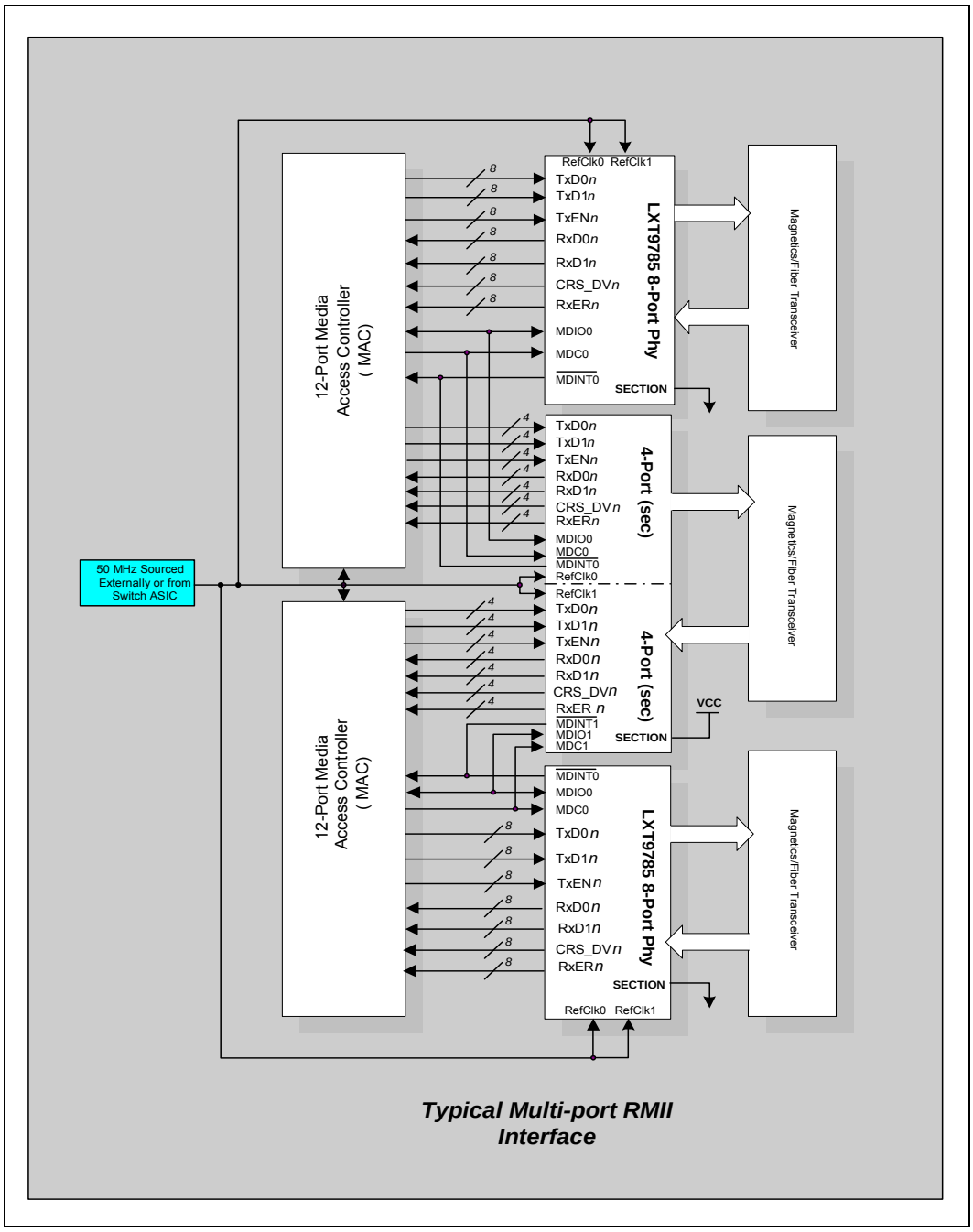


Figure 5 LXT9785/LXT9785E Transceiver Typical SMII Quad Sectionalization Diagram

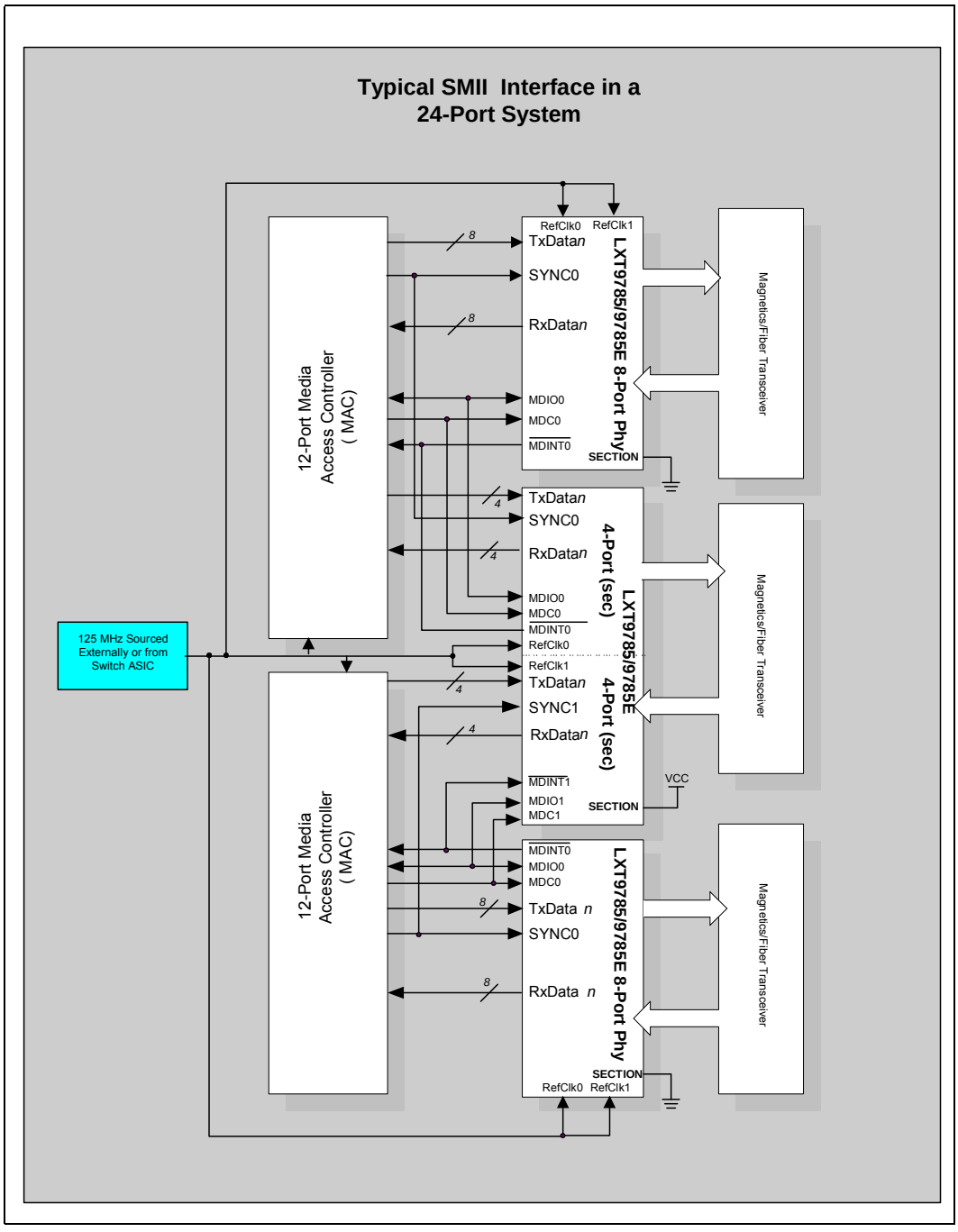
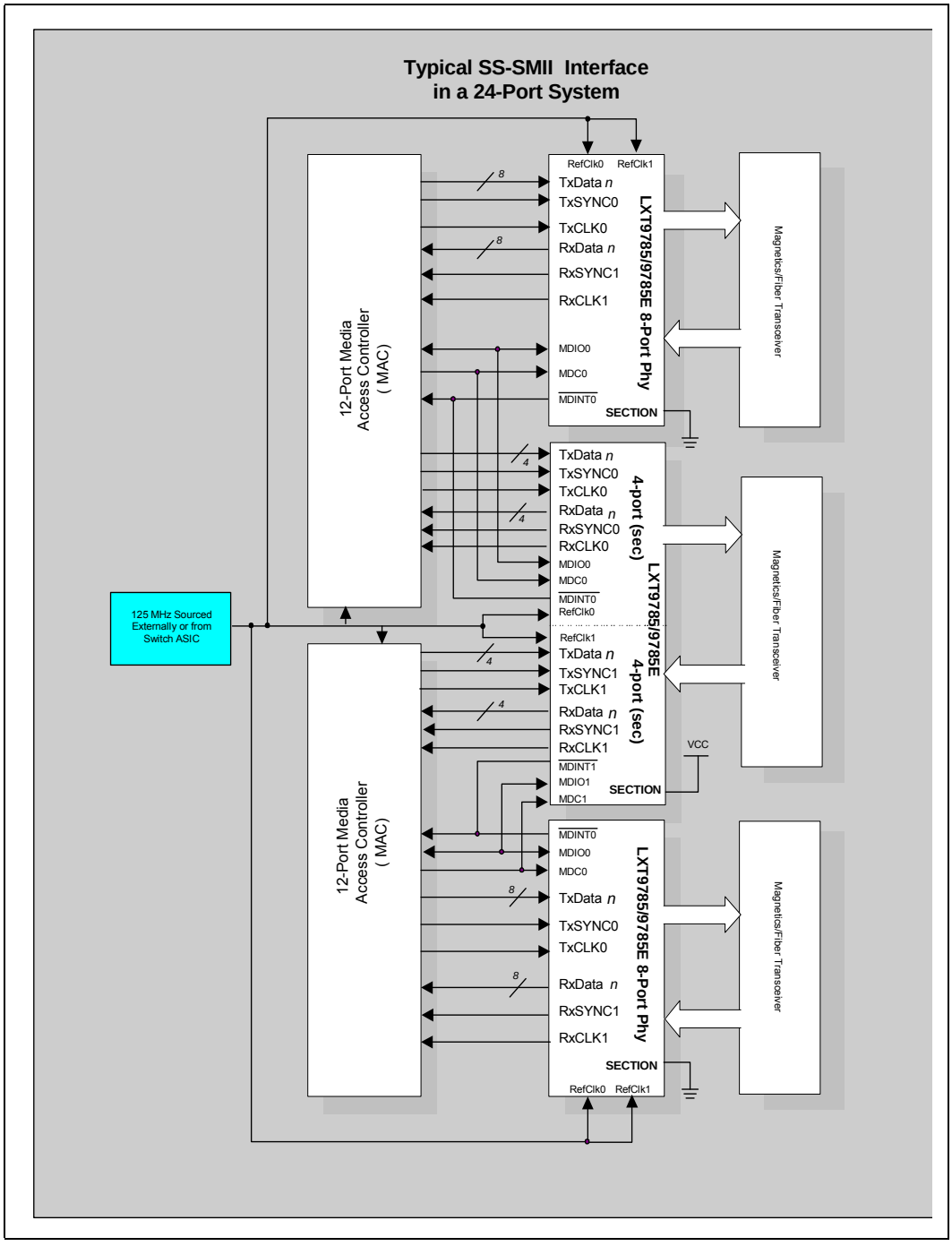


Figure 6 LXT9785/LXT9785E Transceiver Typical SS-SMII Quad Sectionalization Diagram



4.2 Mode Controls and Indicators

Both the LXT9784 Transceiver and LXT9785/LXT9785E Transceiver support applications that use either Manual/Hardware control or MDIO/Software control. The design upgrade from the LXT9784 Transceiver to the LXT9785/LXT9785E Transceiver is relatively simple. Table 3 provides a hardware/software control mode comparison.

Table 3 Hardware/Software Control Mode Comparison

Mode	Configuration	
	LXT9784 Transceiver	LXT9785/LXT9785E Transceiver
Manual/Hardware Control Mode Both devices have identical settings. Refer to Table 4 for a comparison.		
MDDIS	Not supported	The operation of a physical interface consisting of a data line (MDIO) and clock line (MDC) is controlled by the MDDIS input pin. When MDDIS is Low, the MDIO port is enabled for both read and write operations. When MDDIS is High, only the Write operation is disabled on the MDIO bus.
MDIO/Software Control Mode Both devices support the IEEE 802.3 MDIO Management Interface.		
Clock Speed	Requires an external clock (MDC) to drive the MDIO interface.	Same
	Clock speed up to 3 MHz.	Clock speed has been increased up to 20 MHz to allow for faster control interface circuits.
REFCLK	Requires a constant 50 MHz (RMII) and 125 MHz (SMII) reference clock that must be enabled at all times.	Same

4.3 Hardware Configuration Settings

Table 4 provides the hardware configuration settings for the LXT9785/LXT9785E Transceiver. The LXT9784 Transceiver does not support the CFG pin feature.

Table 4 Hardware Configuration Settings for LXT9785/LXT9785E Transceiver

Desired Mode			LXT9785/LXT9785E Transceiver CFG Pin Settings		
Auto-Neg	**Speed**	**Duplex**	**CFG1**	**CFG2**	**CFG3**
Disabled	10	Half	Low	Low	Low
		Full	Low	Low	High
	100	Half	Low	High	Low
		Full	Low	High	High
Enabled	100 Only	Half	High	Low	Low
		Full	High	Low	High
	10/100	Half Only	High	High	Low
		Full or Half	High	High	High

1. The LXT9785/LXT9785E Transceiver use one set of global pins per device. Refer to the LXT9785/LXT9785E Transceiver (document number 249241) and LXT9784 Transceiver (document number 249272) Datasheets for detailed information.

The LXT9784 Transceiver has three LED pins per port dedicated to driving the LED signals. Unlike the LXT9785/LXT9785E Transceiver, all three LEDs can only be selected via the register of each port of the LXT9784 Transceiver. Table 5 provides LED functionality for the LXT9784 Transceiver.

Table 5 LED Functionality

LED driver	Function	Description
$\overline{\text{LEDn\_A}}$	Link = solid Activity = blink	With a good link, the output is Low. The output toggles at a rate related to the utilization.
$\overline{\text{LEDn\_B}}$	Speed	The output is Low for 100 Mbps and High for 10 Mbps
$\overline{\text{LEDn\_C}}$	Collision	The output blinks low with a collision stretch rate of 10 ms.

1. *n* indicates port number.

4.4 RMII, SMII, and SS-SMII Interfaces

The RMII and SMII interfaces for the LXT9784 Transceiver and LXT9785/LXT9785E Transceiver are compared in Table 6. The LXT9785/LXT9785E Transceiver also supports an SS-SMII interface, which is not supported by the LXT9784 Transceiver.

Table 6 Switch Interface Comparison

Feature	LXT9784 Transceiver	LXT9785/LXT9785E Transceiver
RMII and SMII Interfaces		
Switch Interfaces	RMII and SMII interface for each network port SS-SMII not supported	RMII, SMII, and SS-SMII Refer to Figure 6, *LXT9785/LXT9785E Transceiver Typical SS-SMII Quad Sectionalization Diagram*, on page 14 for an illustration of the SS-SMII interface
Sectionalization	Not Supported.	Allows the device to be sectionalized into 1x8 or 2x4 (two quad sections). The MDIO, switch interface, and ref clock are split into two separate PHY interfaces (see Figure 4, Figure 5, and Figure 6).
MII Interrupts	Provides two dedicated interrupt registers for each port. Register 18 of each PHY provides interrupt enable and Register 19 provides interrupt status. Setting Register bit 18.1 = 1 of each PHY enables a port to request interrupt via the MDINT pin. An active low on this pin indicates a status change on each PHY. Interrupts may be caused by any of the following conditions for each PHY:	Same
	• Auto-Negotiation Complete • Speed Status Change • Duplex Status Change • Link Status Change • Isolate Status Change	Same

4.5 Register Sets

Table 7 provides a comparison of Register Sets. Refer to the LXT9784 Transceiver and LXT9785/LXT9785E Transceiver datasheets for comprehensive information on register sets.

Table 7 LXT9784 Transceiver-to-LXT9785/LXT9785E Transceiver Register Set Comparison

Register Address	LXT9784 Transceiver	LXT9785/LXT9785E Transceiver (RMII Mode)
0	Control Register	Same
1	Status Register	Same
2	PHY Identification Register 1	Same
3	PHY Identification Register 2	Same
4	Auto-Negotiation Advertisement Register	Same
5	Auto-Negotiation Link Partner Base Page Ability Register	Same
6	Auto-Negotiation Expansion Register	Same
7	Reserved	Auto-Negotiation Next Page Transmit Register
8	Reserved	Auto-Negotiation Link Partner Next Page Receive Register
9 through15	Reserved	Same
16	Status and Control Register	Port Configuration Register
17	Special Control Register	Quick Status Register
18	PHY Interrupt Register	Interrupt Enable Register
19	100BASE-TX RCV False-Carrier Counter Register	Interrupt Status Register
20	100BASE-TX RCV Disconnect Counter Register	LED Configuration Register
21	100BASE-TX RCV Error Frame Counter Register	Receive Error Count Register
22	Received Symbol Error Counter Register	Reserved
23	100BASE-TX RCV Premature End of Frame Register	Reserved
24	1-BASE-T RCV End of Frame Counter Register	Reserved
25	10BASE-T Jabber Detect Counter Register	RMII Out-of-Bank Signaling Register
26	Reserved	Same
27	PHY Special Control	Trim Enable Register
28	MDI/MDIX Control	Reserved
29	Hardware Integrity Control	Reserved
30 through 31	Reserved	Same

4.6 LED Drivers

The LEDs in the LXT9784 Transceiver are not controllable through hardware or software. In the LXT9785/LXT9785E Transceiver, the LED drivers can be programmed to display various combined status conditions. Refer to the LED Configuration Register in the LXT9785/LXT9785E Transceiver Datasheet.

5.0 General

This section covers the following areas:

- Section 5.1, *Power Management*
- Section 5.2, *JTAG Boundary Scan*, on page 20
- Section 5.3, *Package and Temperature Options*, on page 20
- Section 5.4, *Ball Assignments*, on page 20

5.1 Power Management

Table 8 provides a comparison of power supplies, support for lower-voltage MACs, power-down mode, and transmit driver supply for both the LXT9784 Transceiver and LXT9785/ LXT9785E Transceiver.

Table 8 Power Management Comparison

Function	Description	LXT9784 Transceiver	LXT9785/LXT9785E Transceiver
Power Supply			
VCCIO	Digital Power Supply I/O Ring.	3.3 V	2.5 V/3.3 V
VCCD	Digital Power Supply Core.	3.3 V	2.5 V
VCCA	The common power supply for all analog circuits.	3.3 V (including all the transmit and receive circuits plus the magnetics center tap.	2.5 V
GND	Common ground for all supplies.	Same	Same
VCCPECL	Digital power supply - PECL Signal Detect Inputs.	Not supported.	2.5 V/3.3 V supply for PECL signal detect input circuits. When fiber mode is not used, these pins are tied to GNDPECL to save power.
GNDPECL	Ground return for all PECL Signal Detect Input circuits.	Not supported.	Digital GND. PECL Signal Detect Input.
Support for Lower-Voltage MACs	Power supply input VCCIO supports the MII interface to the MAC controller.	Regardless of the I/O supply, digital I/O pins remain tolerant of 5V signal levels.	Signals are tolerant to 3.3 V/ 5.0 V when the I/O supply is 3.3 V and 2.5 V/3.3 V/5.0 V when the I/O supply is 2.5 V.
Power-Down Mode	Feature to save power.	Supports a power-down mode that is enabled via an external input pin (the hardware global power-down) or per port via the MDIO Control register.	Same
Transmit Driver Supply	External voltage to drive signals.	The LXT9784 Transceiver is a voltage-driven transceiver and does not require an external power supply to drive the output signals	The LXT9785/LXT9785E Transceiver are current-driven transceivers. The driver current can be supplied from an external 3.3 V or 2.5 V source. Using a 2.5 V source provides significant power savings.

5.2 JTAG Boundary Scan

The LXT9785/LXT9785E Transceiver provides a JTAG 1149.1 boundary scan test port, providing direct access to every pin on the device and simplifying production test requirements. The standard requirement for ‘bed of nails’ test fixtures may be eliminated in many applications. This is particularly advantageous for applications using the BGA package.

5.3 Package and Temperature Options

The LXT9785/LXT9785E Transceiver is available in two packages, Plastic Quad Flat Pack (PQFP) and Plastic Ball-Grid Array (PBGA) while the LXT9784 Transceiver is available in a PBGA package only. Both devices support industrial and commercial temperatures.

5.4 Ball Assignments

Table 9 provides a ball-to-ball comparison to assist in design conversions.

Note: The SS-SMII interface ball assignments for the LXT9785/LXT9785E Transceiver are included in Table 9. The LXT9784 Transceiver does not support SS-SMII.

Table 9 LXT9784 Transceiver and LXT9785/LXT9785E Transceiver RMII and SMII BGA Comparison (Sheet 1 of 13)

Ball#	Signal Name				
	RMII		SMII		SS-SMII
	LXT9784 Transceiver	LXT9785/ LXT9785E Transceiver	LXT9784 Transceiver	LXT9785/ LXT9785E Transceiver	LXT9785/ LXT9785E Transceiver
A1	N/C	GNDD	N/C	GNDD	GNDD
A2	TXD7_1	VCCIO	N/C	VCCIO	VCCIO
A3	N/C	RxData1_0	N/C	RxData1	N/C
A4	N/C	TxData2_1	N/C	N/C	N/C
A5	TPON7	CRS_DV2	TPON7	N/C	N/C
A6	TPOP7	TxData3_1	TPOP7	SYNC0	TxSYNC0
A7	N/C	TxEN3	N/C	N/C	N/C
A8	TPON6	VCCIO	TPON6	VCCIO	VCCIO
A9	TPOP6	GNDD	TPOP6	GNDD	GNDD
A10	RBIAS100_1	MDIO1	RBIAS100_1	MDIO1	MDIO1
A11	RBIAS10_1	TxData4_0	RBIAS10_1	TxData4	TxData4
A12	TPON5	RxER4	TPON5	N/C	N/C
A13	TPOP5	RxData4_0	TPOP5	RxData4	N/C
A14	N/C	TxEN5	N/C	N/C	N/C
A15	TPON4	RxER5	TPON4	N/C	N/C
A16	TPOP4	TxData6_1	TPOP4	N/C	N/C

Table 9 LXT9784 Transceiver and LXT9785/LXT9785E Transceiver RMII and SMII BGA Comparison (Sheet 2 of 13)

Ball#	Signal Name				
	RMII		SMII		SS-SMII
	LXT9784 Transceiver	LXT9785/ LXT9785E Transceiver	LXT9784 Transceiver	LXT9785/ LXT9785E Transceiver	LXT9785/ LXT9785E Transceiver
A17	N/C	RxER6	N/C	N/C	N/C
A18	N/C	N/A	N/C	N/A	N/A
A19	N/C	N/A	N/C	N/A	N/A
A20	N/C	N/A	N/C	N/A	N/A
B1	CRSDV7	RxData0_1	N/C	N/C	RxData0
B2	TXEN7	TxEN1	N/C	N/C	N/C
B3	TXD7_0	GNDD	TXD7	GNDD	GNDD
B4	N/C	RxData1_1	N/C	N/C	RxData1
B5	N/C	TxData2_0	N/C	TxData2	TxData2
B6	N/C	RxData2_0	N/C	RxData2	$\overline{\text{N/C}}$
B7	N/C	GNDD	N/C	GNDD	GNDD
B8	N/C	CRS_DV3	N/C	N/C	N/C
B9	N/C	RxData3_1	N/C	N/C	RxData3
B10	VCC	MDC1	VCC	MDC1	MDC1
B11	VCC	TxEN4	VCC	N/C	RxCLK1
B12	N/C	CRS_DV4	N/C	N/C	RxSYNC1
B13	N/C	TxData5_0	N/C	TxData5	TxData5
B14	N/C	RxData5_0	N/C	RxData5	N/C
B15	N/C	RxData5_1	N/C	N/C	RxData5
B16	N/C	CRS_DV6	N/C	N/C	N/C
B17	N/C	RXD6_1	N/C	N/C	RxData6
B18	$\overline{\text{INT}}$	N/A	$\overline{\text{INT}}$	N/A	N/A
B19	MDC	N/A	MDC	N/A	N/A
B20	TOUT	N/A	TOUT	N/A	N/A
C1	RXD6_0	VCCIO	RXD6	VCCIO	VCCIO
C2	RXD7_0	RXD0_0	RXD7	RxData0	RxData0
C3	RXD7_1	TXD1_0	N/C	TxData1	TxData1
C4	N/C	CRS_DV1	N/C	N/C	N/C
C5	TPIN7	GNDD	TPIN7	GNDD	GNDD
C6	TPIP7	TxEN2	TPIP7	N/C	N/C
C7	N/C	RxData2_1	N/C	N/C	RxData2
C8	TPIN6	RxER3	TPIN6	N/C	TxCLK0
C9	TPIP6	$\overline{\text{MDINT1}}$	TPIP6	$\overline{\text{MDINT1}}$	$\overline{\text{MDINT1}}$
C10	GND	TxData4_1	GND	N/C	N/C

Table 9 LXT9784 Transceiver and LXT9785/LXT9785E Transceiver RMII and SMII BGA Comparison (Sheet 3 of 13)

Ball#	Signal Name				
	RMII		SMII		SS-SMII
	LXT9784 Transceiver	LXT9785/ LXT9785E Transceiver	LXT9784 Transceiver	LXT9785/ LXT9785E Transceiver	LXT9785/ LXT9785E Transceiver
C11	GND	VCCIO	GND	VCCIO	VCCIO
C12	TPIN5	RxData4_1	TPIN5	N/C	RxData4
C13	TPIP5	GNDD	TPIP5	GNDD	GNDD
C14	N/C	TxEN6	N/C	N/C	N/C
C15	TPIN4	RxData6_0	TPIN4	RxData6	N/C
C16	TPIP4	TxData7_1	TPIP4	SYNC1	TxSYNC1
C17	N/C	GNDD	N/C	GNDD	GNDD
C18	$\overline{\text{LED7\_B}}$	N/A	$\overline{\text{LED7\_B}}$	N/A	N/A
C19	$\overline{\text{LED7\_A}}$	N/A	$\overline{\text{LED7\_A}}$	N/A	N/A
C20	MDIO	N/A	MDIO	N/A	N/A
D1	TXEN6	GNDD	N/C	GNDD	GNDD
D2	CRSDV6	RxER0/MDIX	N/C	MDIX	MDIX
D3	RXD6_1	GNDD	N/C	GNDD	GNDD
D4	N/C	TxData1_1	N/C	N/C	N/C
D5	GND	RxER1/PAUSE	GND	PAUSE	PAUSE
D6	VCCR	GNDD	VCCR	GNDD	GNDD
D7	N/C	RxER2	N/C	N/C	N/C
D8	GND	TxData3_0	GND	TxData3	TxData3
D9	VCCR	RxData3_0	VCCR	RxData3	N/C
D10	VCC	GNDD	VCC	GNDD	GNDD
D11	GND	TxData5_1	GND	N/C	N/C
D12	GND	CRS_DV5	GND	N/C	N/C
D13	VCCR	TxData6_0	VCCR	TxData6	TxData6
D14	N/C	VCCIO	N/C	VCCIO	VCCIO
D15	GND	GNDD	GND	GNDD	GNDD
D16	VCCR	TxEN7	VCCR	N/C	N/C
D17	N/C	RxER7	N/C	N/C	TxCLK1
D18	$\overline{\text{LED6\_B}}$	N/A	$\overline{\text{LED6\_B}}$	N/A	N/A
D19	$\overline{\text{LED6\_A}}$	N/A	$\overline{\text{LED6\_A}}$	N/A	N/A
D20	$\overline{\text{LED7\_C}}$	N/A	$\overline{\text{LED7\_C}}$	N/A	N/A
E1	TXD5_1	MDC0	N/C	MDC0	MDC0
E2	TXD6_1	TxData0_0	N/C	TxData0	TXD0
E3	TXD6_0	TxEN0	TXD6	N/C	RxCLK0
E4	VCCIO	CRS_DV0	VCCIO	N/C	RxSYNC0

Table 9 LXT9784 Transceiver and LXT9785/LXT9785E Transceiver RMII and SMII BGA Comparison (Sheet 4 of 13)

Ball#	Signal Name				
	RMII		SMII		SS-SMII
	LXT9784 Transceiver	LXT9785/ LXT9785E Transceiver	LXT9784 Transceiver	LXT9785/ LXT9785E Transceiver	LXT9785/ LXT9785E Transceiver
E5	GND	GNDD	GND	GNDD	GNDD
E6	VCC	REFCLK0	VCC	REFCLK0	REFCLK0
E7	GND	GNDD	GND	GNDD	GNDD
E8	GND	–	GND	–	–
E9	VCC	GNDD	VCC	GNDD	GNDD
E10	GND	–	GND	–	–
E11	GND	GNDD	GND	GNDD	GNDD
E12	GND	REFCLK1	GND	REFCLK1	REFCLK1
E13	VCC	GNDD	VCC	GNDD	GNDD
E14	GND	TXD7_0	GND	TxData7	TxData7
E15	GND	CRS_DV7	GND	N/C	N/C
E16	VCC	RxData7_0	VCC	RxData7	N/C
E17	VCCIO	GNDD	VCCIO	GNDD	GNDD
E18	$\overline{\text{LED5\_B}}$	N/A	$\overline{\text{LED5\_B}}$	N/A	N/A
E19	$\overline{\text{LED5\_A}}$	N/A	$\overline{\text{LED5\_A}}$	N/A	N/A
E20	$\overline{\text{LED6\_C}}$	N/A	$\overline{\text{LED6\_C}}$	N/A	N/A
F1	CRSDV5	$\overline{\text{MDINT0}}$	N/C	$\overline{\text{MDINT0}}$	$\overline{\text{MDINT0}}$
F2	TXEN5	$\overline{\text{LED3\_1}}$	N/C	$\overline{\text{LED3\_1}}$	$\overline{\text{LED3\_1}}$
F3	TXD5_0	MDIO0	TXD5	MDIO0	MDIO0
F4	GND	$\overline{\text{TxData0\_1}}$	GND	N/C	N/C
F5	N/C	VCCD	N/C	VCCD	VCCD
F6	N/C	–	N/C	–	–
F7	–	–	–	–	–
F8	–	–	–	–	–
F9	–	–	–	–	–
F10	–	–	–	–	–
F11	–	–	–	–	–
F12	–	–	–	–	–
F13	–	GNDD	–	GNDD	GNDD
F14	N/C	RXD7_1	–	N/C	RxData7
F15	N/C	N/C	–	$\overline{\text{N/C}}$	N/C
F16	N/C	$\overline{\text{LED7\_3}}$	–	$\overline{\text{LED7\_3}}$	$\overline{\text{LED7\_3}}$
F17	GND	$\overline{\text{LED7\_2}}$	GND	$\overline{\text{LED7\_2}}$	$\overline{\text{LED7\_2}}$
F18	$\overline{\text{LED4\_B}}$	N/A	$\overline{\text{LED4\_B}}$	N/A	N/A

Table 9 LXT9784 Transceiver and LXT9785/LXT9785E Transceiver RMII and SMII BGA Comparison (Sheet 5 of 13)

Ball#	Signal Name				
	RMII		SMII		SS-SMII
	LXT9784 Transceiver	LXT9785/ LXT9785E Transceiver	LXT9784 Transceiver	LXT9785/ LXT9785E Transceiver	LXT9785/ LXT9785E Transceiver
F19	LED4_A	N/A	LED4_A	N/A	N/A
F20	LED5_C	N/A	LED5_C	N/A	N/A
G1	RXD4_0	LED2_3	RXD4	LED2_3	LED2_3
G2	RXD5_0	N/C	RXD5	N/C	N/C
G3	RXD5_1	LED3_2	N/C	LED3_2	LED3_2
G4	VCCIO	LED3_3	VCCIO	LED3_3	LED3_3
G5	VCC	N/C	VCC	N/C	N/C
G6	N/C	–	N/C	–	–
G7	–	–	–	–	–
G8	–	–	–	–	–
G9	–	–	–	–	–
G10	–	–	–	–	–
G11	–	–	–	–	–
G12	–	–	–	–	–
G13	–	VCCD	–	VCCD	VCCD
G14	–	N/C	–	N/C	N/C
G15	–	LED7_1	–	LED7_1	LED7_1
G16	VCC	N/C	VCC	N/C	N/C
G17	VCCIO	LED6_3	VCCIO	LED6_3	LED6_3
G18	MDIX	N/A	MDIX	N/A	N/A
G19	LED3_A	N/A	LED3_A	N/A	N/A
G20	LED4_C	N/A	LED4_C	N/A	N/A
H1	TXEN4	LED1_3	N/C	LED1_3	LED1_3
H2	CRSDV4	LED2_1	N/C	LED2_1	LED2_1
H3	RXD4_1	LED2_2	N/C	LED2_2	LED2_2
H4	GND	N/C	GND	N/C	N/C
H5	VCC	–	VCC	–	–
H6	–	–	–	–	–
H7	–	–	–	–	–
H8	–	GNDD	–	GNDD	GNDD
H9	–	GNDD	–	GNDD	GNDD
H10	–	GNDD	–	GNDD	GNDD
H11	–	–	–	–	–
H12	–	–	–	–	–

Table 9 LXT9784 Transceiver and LXT9785/LXT9785E Transceiver RMII and SMII BGA Comparison (Sheet 6 of 13)

Ball#	Signal Name				
	RMII		SMII		SS-SMII
	LXT9784 Transceiver	LXT9785/ LXT9785E Transceiver	LXT9784 Transceiver	LXT9785/ LXT9785E Transceiver	LXT9785/ LXT9785E Transceiver
H13	–	–	–	–	–
H14	–	N/C	–	N/C	N/C
H15	–	LED6_1	–	LED6_1	LED6_1
H16	VCC	LED6_2	VCC	LED6_2	LED6_2
H17	GND	LED5_3	GND	LED5_3	LED5_3
H18	TEXEC	N/A	TEXEC	N/A	N/A
H19	TI	N/A	TI	N/A	N/A
H20	TCK	N/A	TCK	N/A	N/A
J1	MODE_0	LED0_3	MODE_0	LED0_3	LED0_3
J2	TXD4_1	N/C	N/C	N/C	N/C
J3	TXD4_0	LED1_2	TXD4	LED1_2	LED1_2
J4	VCCIO	LED1_1	VCCIO	LED1_1	LED1_1
J5	VCC	VCCD	VCC	VCCD	VCCD
J6	–	–	–	–	–
J7	–	–	–	–	–
J8	–	GNDD	–	GNDD	GNDD
J9	GND	GNDD	GND	GNDD	GNDD
J10	GND	GNDD	GND	GNDD	GNDD
J11	GND	–	GND	–	–
J12	GND	–	GND	–	–
J13	–	N/C	–	N/C	N/C
J14	–	VCCD	–	VCCD	VCCD
J15	–	LED5_1	–	LED5_1	LED5_1
J16	VCC	LED5_2	VCC	LED5_2	LED5_2
J17	VCC	LED4_3	VCC	LED4_3	LED4_3
J18	N/C	N/A	N/C	N/A	N/A
J19	N/C	N/A	N/C	N/A	N/A
J20	N/C	N/A	N/C	N/A	N/A
K1	FRCLNK	AMDIX_EN	FRCLNK	AMDIX_EN	AMDIX_EN
K2	MODE_1	LED0_2	MODE_1	LED0_2	LED0_2
K3	MCLK	LED0_1	MCLK	LED0_1	LED0_1
K4	GND	N/C	GND	N/C	N/C
K5	VCC	–	VCC	–	–
K6	–	–	–	–	–

Table 9 LXT9784 Transceiver and LXT9785/LXT9785E Transceiver RMII and SMII BGA Comparison (Sheet 7 of 13)

Ball#	Signal Name				
	RMII		SMII		SS-SMII
	LXT9784 Transceiver	LXT9785/ LXT9785E Transceiver	LXT9784 Transceiver	LXT9785/ LXT9785E Transceiver	LXT9785/ LXT9785E Transceiver
K7	–	–	–	–	–
K8	–	GNDD	–	GNDD	GNDD
K9	GND	GNDD	GND	GNDD	GNDD
K10	GND	GNDD	GND	GNDD	GNDD
K11	GND	–	GND	–	–
K12	GND	–	GND	–	–
K13	–	–	–	–	–
K14	–	SGND	–	SGND	SGND
K15	–	N/C	–	N/C	N/C
K16	VCC	$\overline{\text{LED4\_1}}$	VCC	$\overline{\text{LED4\_1}}$	$\overline{\text{LED4\_1}}$
K17	GND	$\overline{\text{LED4\_2}}$	GND	$\overline{\text{LED4\_2}}$	$\overline{\text{LED4\_2}}$
K18	RESET	N/A	RESET	N/A	N/A
K19	BP4B5B	N/A	BP4B5B	N/A	N/A
K20	SCRMBP	N/A	SCRMBP	N/A	N/A
L1	TXD4	MDDIS	SYNC	MDDIS	MDDIS
L2	MODE_2	CFG_3	MODE_2	CFG_3	CFG_3
L3	FRC34	CFG_2	FRC34	CFG_2	CFG_2
L4	VCCIO	ADD_4	VCCIO	ADD_4	ADD_4
L5	VCC	VCCPECL	VCC	VCCPECL	VCCPECL
L6	–	–	–	–	–
L7	–	–	–	–	–
L8	–	–	–	–	–
L9	GND	–	GND	–	–
L10	GND	–	GND	–	–
L11	GND	–	GND	–	–
L12	GND	–	GND	–	–
L13	–	VCCPECL	–	VCCPECL	VCCPECL
L14	–	PWRDWN	–	PWRDWN	PWRDWN
L15	–	SECTION	–	SECTION	SECTION
L16	VCC	MODESEL_0	VCC	MODESEL_0	MODESEL_0
L17	VCCIO	MODESEL_1	VCCIO	MODESEL_1	MODESEL_1
L18	RXER0	N/A	N/C	N/A	N/A
L19	ID_1	N/A	ID_1	N/A	N/A
L20	ID_0	N/A	ID_0	N/A	N/A

Table 9 LXT9784 Transceiver and LXT9785/LXT9785E Transceiver RMII and SMII BGA Comparison (Sheet 8 of 13)

Ball#	Signal Name				
	RMII		SMII		SS-SMII
	LXT9784 Transceiver	LXT9785/ LXT9785E Transceiver	LXT9784 Transceiver	LXT9785/ LXT9785E Transceiver	LXT9785/ LXT9785E Transceiver
M1	TXEN3	CFG_1	N/C	CFG_1	CFG_1
M2	TXD3_0	ADD_3	TXD3	ADD_3	ADD_3
M3	TXD3_1	ADD_2	N/C	ADD_2	ADD_2
M4	GND	TxSLEW_1	GND	TxSLEW_1	TxSLEW_1
M5	VCC	GNDPECL	VCC	GNDPECL	GNDPECL
M6	–	–	–	–	–
M7	–	–	–	–	–
M8	–	–	–	–	–
M9	GND	–	GND	–	–
M10	GND	–	GND	–	–
M11	GND	–	GND	–	–
M12	GND	–	GND	–	–
M13	–	GNDPECL	–	GNDPECL	GNDPECL
M14	–	G_FX/$\overline{TP}$	–	G_FX/$\overline{TP}$	G_FX/$\overline{TP}$
M15	–	$\overline{RESET}$	–	$\overline{RESET}$	$\overline{RESET}$
M16	VCC	TCK	VCC	TCK	TCK
M17	GND	$\overline{TRST}$	GND	$\overline{TRST}$	$\overline{TRST}$
M18	RXER3	N/A	RXER3	N/A	N/A
M19	RXER2	N/A	RXER2	N/A	N/A
M20	RXER1	N/A	RXER1	N/A	N/A
N1	RXD3_0	ADD_1	RXD3	ADD_1	ADD_1
N2	RXD3_1	ADD_0	N/C	ADD_0	ADD_0
N3	CRSDV3	TxSLEW_0	N/C	TxSLEW_0	TxSLEW_0
N4	VCCIO	SD1	VCCIO	SD1	SD1
N5	VCC	SD3	VCC	SD3	SD3
N6	–	VCCT	–	VCCT	VCCT
N7	–	VCCT	–	VCCT	VCCT
N8	–	–	–	–	–
N9	–	VCCT	–	VCCT	VCCT
N10	–	–	–	–	–
N11	–	VCCT	–	VCCT	VCCT
N12	–	VCCT	–	VCCT	VCCT
N13	–	VCCR	–	VCCR	VCCR
N14	–	TDI	–	TDI	TDI

Table 9 LXT9784 Transceiver and LXT9785/LXT9785E Transceiver RMII and SMII BGA Comparison (Sheet 9 of 13)

Ball#	Signal Name				
	RMII		SMII		SS-SMII
	LXT9784 Transceiver	LXT9785/ LXT9785E Transceiver	LXT9784 Transceiver	LXT9785/ LXT9785E Transceiver	LXT9785/ LXT9785E Transceiver
N15	–	TDO	–	TDO	TDO
N16	VCC	TMS	VCC	TMS	TMS
N17	VCCIO	SD7	VCCIO	SD7	SD7
N18	RXER6	N/A	N/C	N/A	N/A
N19	RXER5	N/A	N/C	N/A	N/A
N20	RXER4	N/A	N/C	N/A	N/A
P1	CRSDV2	SD_2P5V	N/C	SD_2P5V	SD_2P5V
P2	RXD2_1	SD0	N/C	SD0	SD0
P3	RXD2_0	SD2	RXD2	SD2	SD2
P4	GND	VCCR	GND	VCCR	VCCR
P5	VCC	GNDR	VCC	GNDR	GNDR
P6	–	GNDR	–	GNDR	GNDR
P7	–	VCCR	–	VCCR	VCCR
P8	–	VCCR	–	VCCR	VCCR
P9	–	VCCR	–	VCCR	VCCR
P10	–	VCCR	–	VCCR	VCCR
P11	–	VCCR	–	VCCR	VCCR
P12	–	VCCR	–	VCCR	VCCR
P13	–	GNDR	–	GNDR	GNDR
P14	–	GNDT	–	GNDT	GNDT
P15	N/C	SD4	N/C	SD4	SD4
P16	VCC	SD5	VCC	SD5	SD5
P17	GND	SD6	GND	SD6	SD6
P18	$\overline{\text{LED3\_C}}$	N/A	$\overline{\text{LED3\_C}}$	N/A	N/A
P19	$\overline{\text{LED3\_B}}$	N/A	$\overline{\text{LED3\_B}}$	N/A	N/A
P20	RXER7	N/A	RXER7	N/A	N/A
R1	TXD2_1	GNDT	N/C	GNDT	GNDT
R2	TXD2_0	TPFIP(0)	TXD2	TPFIP(0)	TPFIP(0)
R3	TXEN2	GNDT	N/C	GNDT	GNDT
R4	VCCIO	TPFON(1)	VCCIO	TPFON(1)	TPFON(1)
R5	N/C	GNDT	N/C	GNDT	GNDT
R6	N/C	TPFIP(2)	N/C	TPFIP(2)	TPFIP(2)
R7	N/C	GNDR	N/C	GNDR	GNDR
R8	–	TPFIN(3)	–	TPFIN(3)	TPFIN(3)

Table 9 LXT9784 Transceiver and LXT9785/LXT9785E Transceiver RMII and SMII BGA Comparison (Sheet 10 of 13)

Ball#	Signal Name				
	RMII		SMII		SS-SMII
	LXT9784 Transceiver	LXT9785/ LXT9785E Transceiver	LXT9784 Transceiver	LXT9785/ LXT9785E Transceiver	LXT9785/ LXT9785E Transceiver
R9	–	GNDR	–	GNDR	GNDR
R10	–	TPFON(4)	–	TPFON(4)	TPFON(4)
R11	–	GNDR	–	GNDR	GNDR
R12	–	TPFIP(6)	–	TPFIP(6)	TPFIP(6)
R13	–	GNDR	–	GNDR	GNDR
R14	–	TPFOP(7)	–	TPFOP(7)	TPFOP(7)
R15	N/C	GNDT	N/C	GNDT	GNDT
R16	N/C	TPFIP(7)	N/C	TPFIP(7)	TPFIP(7)
R17	VCCIO	GNDT	VCCIO	GNDT	GNDT
R18	$\overline{\text{LED2\_C}}$	N/A	$\overline{\text{LED2\_C}}$	N/A	N/A
R19	$\overline{\text{LED2\_B}}$	N/A	$\overline{\text{LED2\_B}}$	N/A	N/A
R20	$\overline{\text{LED2\_A}}$	N/A	$\overline{\text{LED2\_A}}$	N/A	N/A
T1	TXEN1	TPFIN(0)	N/C	TPFIN(0)	TPFIN(0)
T2	TXD1_0	TPFOP(0)	TXD1	TPFOP(0)	TPFOP(0)
T3	TXD1_1	TPFOP(1)	N/C	TPFOP(1)	TPFOP(1)
T4	GND	TPFIN(1)	GND	TPFIN(1)	TPFIN(1)
T5	GND	TPFIN(2)	GND	TPFIN(2)	TPFIN(2)
T6	VCC	TPFOP(2)	VCC	TPFOP(2)	TPFOP(2)
T7	GND	TPFON(3)	GND	TPFON(3)	TPFON(3)
T8	GND	TPFIP(3)	GND	TPFIP(3)	TPFIP(3)
T9	VCC	TPFIP(4)	VCC	TPFIP(4)	TPFIP(4)
T10	GND	TPFOP(4)	GND	TPFOP(4)	TPFOP(4)
T11	GND	TPFOP(5)	GND	TPFOP(5)	TPFOP(5)
T12	GND	TPFIN(5)	GND	TPFIN(5)	TPFIN(5)
T13	VCC	TPFIN(6)	VCC	TPFIN(6)	TPFIN(6)
T14	GND	TPFOP(6)	GND	TPFOP(6)	TPFOP(6)
T15	GND	TPFON(7)	GND	TPFON(7)	TPFON(7)
T16	VCC	TPFIN(7)	VCC	TPFIN(7)	TPFIN(7)
T17	GND	GNDT	GND	GNDT	GNDT
T18	$\overline{\text{LED1\_C}}$	N/A	$\overline{\text{LED1\_C}}$	N/A	N/A
T19	$\overline{\text{LED1\_B}}$	N/A	$\overline{\text{LED1\_B}}$	N/A	N/A
T20	$\overline{\text{LED1\_A}}$	N/A	$\overline{\text{LED1\_A}}$	N/A	N/A
U1	RXD1_0	TPFON(0)	RXD1	TPFON(0)	TPFON(0)
U2	RXD1_1	GNDT	N/C	GNDT	GNDT

Table 9 LXT9784 Transceiver and LXT9785/LXT9785E Transceiver RMII and SMII BGA Comparison (Sheet 11 of 13)

Ball#	Signal Name				
	RMII		SMII		SS-SMII
	LXT9784 Transceiver	LXT9785/ LXT9785E Transceiver	LXT9784 Transceiver	LXT9785/ LXT9785E Transceiver	LXT9785/ LXT9785E Transceiver
U3	CRSDV1	TPFIP(1)	N/C	TPFIP(1)	TPFIP(1)
U4	N/C	GNDT	N/C	GNDT	GNDT
U5	GND	TPFON(2)	GND	TPFON(2)	TPFON(2)
U6	VCCR	GNDT	VCCR	GNDT	GNDT
U7	N/C	TPFOP(3)	N/C	TPFOP(3)	TPFOP(3)
U8	GND	GNDR	GND	GNDR	GNDR
U9	VCCR	TPFIN(4)	VCCR	TPFIN(4)	TPFIN(4)
10	VCC	GNDT	VCC	GNDT	GNDT
U11	GND	TPFON(5)	GND	TPFON(5)	TPFON(5)
U12	GND	GNDT	GND	GNDT	GNDT
U13	VCCR	TPFIP(5)	VCCR	TPFIP(5)	TPFIP(5)
U14	N/C	GNDT	N/C	GNDT	GNDT
U15	GND	TPFON(6)	GND	TPFON(6)	TPFON(6)
U16	VCCR	GNDT	VCCR	GNDT	GNDT
U17	N/C	GNDT	N/C	GNDT	GNDT
U18	$\overline{\text{LED0\_C}}$	N/A	$\overline{\text{LED0\_C}}$	N/A	N/A
U19	$\overline{\text{LED0\_B}}$	N/A	$\overline{\text{LED0\_B}}$	N/A	N/A
U20	$\overline{\text{LED0\_A}}$	N/A	$\overline{\text{LED0\_A}}$	N/A	N/A
V1	CRSDV0	N/A	N/C	N/A	N/A
V2	RXD0_1	N/A	N/C	N/A	N/A
V3	RXD0_0	N/A	RXD0	N/A	N/A
V4	N/C	N/A	N/C	N/A	N/A
V5	TPIP0	N/A	TPIP0	N/A	N/A
V6	TPIN0	N/A	TPIN0	N/A	N/A
V7	N/C	N/A	N/C	N/A	N/A
V8	TPIP1	N/A	TPIP1	N/A	N/A
V9	TPIN1	N/A	TPIN1	N/A	N/A
V10	GND	N/A	GND	N/A	N/A
V11	GND	N/A	GND	N/A	N/A
V12	TPIP2	N/A	TPIP2	N/A	N/A
V13	TPIN2	N/A	TPIN2	N/A	N/A
V14	N/C	N/A	N/C	N/A	N/A
V15	TPIP3	N/A	TPIP3	N/A	N/A
V16	TPIN3	N/A	TPIN3	N/A	N/A

Table 9 LXT9784 Transceiver and LXT9785/LXT9785E Transceiver RMII and SMII BGA Comparison (Sheet 12 of 13)

Ball#	Signal Name				
	RMII		SMII		SS-SMII
	LXT9784 Transceiver	LXT9785/ LXT9785E Transceiver	LXT9784 Transceiver	LXT9785/ LXT9785E Transceiver	LXT9785/ LXT9785E Transceiver
V17	N/C	N/A	N/C	N/A	N/A
V18	N/C	N/A	N/C	N/A	N/A
V19	N/C	N/A	N/C	N/A	N/A
V20	N/C	N/A	N/C	N/A	N/A
W1	TXD0_1	N/A	N/C	N/A	N/A
W2	TXD0_0	N/A	TXD0	N/A	N/A
W3	TXEN0	N/A	N/C	N/A	N/A
W4	N/C	N/A	N/C	N/A	N/A
W5	N/C	N/A	N/C	N/A	N/A
W6	N/C	N/A	N/C	N/A	N/A
W7	N/C	N/A	N/C	N/A	N/A
W8	N/C	N/A	N/C	N/A	N/A
W9	N/C	N/A	N/C	N/A	N/A
W10	VCC	N/A	VCC	N/A	N/A
W11	VCC	N/A	VCC	N/A	N/A
W12	N/C	N/A	N/C	N/A	N/A
W13	N/C	N/A	N/C	N/A	N/A
W14	N/C	N/A	N/C	N/A	N/A
W15	N/C	N/A	N/C	N/A	N/A
W16	N/C	N/A	N/C	N/A	N/A
W17	N/C	N/A	N/C	N/A	N/A
W18	N/C	N/A	N/C	N/A	N/A
W19	N/C	N/A	N/C	N/A	N/A
W20	N/C	N/A	N/C	N/A	N/A
Y1	N/C	N/A	N/C	N/A	N/A
Y2	N/C	N/A	N/C	N/A	N/A
Y3	N/C	N/A	N/C	N/A	N/A
Y4	N/C	N/A	N/C	N/A	N/A
Y5	TPOP0	N/A	TPOP0	N/A	N/A
Y6	TPON0	N/A	TPON0	N/A	N/A
Y7	N/C	N/A	N/C	N/A	N/A
Y8	TPOP1	N/A	TPOP1	N/A	N/A
Y9	TPON1	N/A	TPON1	N/A	N/A
Y10	RBIAS100_0	N/A	RBIAS100_0	N/A	N/A

Table 9 LXT9784 Transceiver and LXT9785/LXT9785E Transceiver RMII and SMII BGA Comparison (Sheet 13 of 13)

Ball#	Signal Name				
	RMII		SMII		SS-SMII
	LXT9784 Transceiver	LXT9785/ LXT9785E Transceiver	LXT9784 Transceiver	LXT9785/ LXT9785E Transceiver	LXT9785/ LXT9785E Transceiver
Y11	RBIAS10_0	N/A	RBIAS10_0	N/A	N/A
Y12	TPOP2	N/A	TPOP2	N/A	N/A
Y13	TPON2	N/A	TPON2	N/A	N/A
Y14	N/C	N/A	N/C	N/A	N/A
Y15	TPOP3	N/A	TPOP3	N/A	N/A
Y16	TPON3	N/A	TPON3	N/A	N/A
Y17	N/C	N/A	N/C	N/A	N/A
Y18	N/C	N/A	N/C	N/A	N/A
Y19	N/C	N/A	N/C	N/A	N/A
Y20	N/C	N/A	N/C	N/A	N/A

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