# Cortina Systems® 100BASE-FX Fiber Optic Transceivers: Connecting a PECL / LVPECL Interface

## Application Note

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# Revision History

| Revision 2.0<br>Revision Date: 29 March 2007 |
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# 1.0 Introduction

## 1.1 Overview

This application note provides detailed information and recommendations for the circuitry used to interface Cortina Systems® 100BASE-FX PHYs with external fiber-optic transceivers.

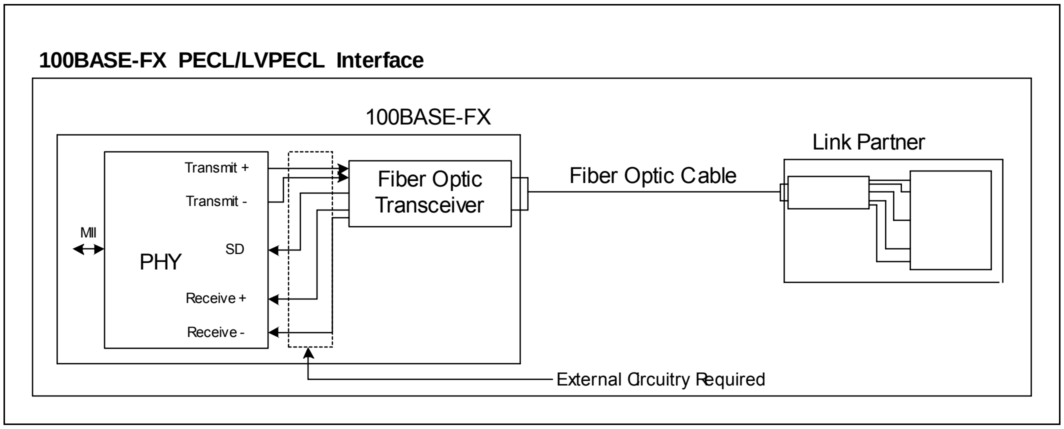
Cortina Systems, Inc. (Cortina) offers IEEE 802.3 compliant 3.3 V and 2.5 V 100BASE-FX Physical Layer products. Fiber-optic transceiver vendors generally offer 5 V and 3.3 V products for 100BASE-FX applications. 5 V devices operate with Positive Emitter Coupled Logic (PECL) signaling levels. 3.3 V and 2.5 V devices operate with Low-Voltage PECL (LVPECL) signaling levels.

The Cortina 100BASE-FX interface consists of a transmit pair and a receive pair, which connect to an external fiber-optic transceiver. A serial 125 Mbaud, 5B-encoded NRZI format is used on the 100BASE-FX interface. Scrambling and MLT-3 coding are not used (as in 100BASE-TX). In addition, most Cortina devices take advantage of the signal detect (SD) feature that many fiber-optic transceivers offer. SD indicates the reception of valid signals from the fiber-optic medium.

**Note:** The Cortina fiber interface is intended for 100BASE-FX applications and does not support 10BASE-FL applications.

The external fiber-optic transceiver provides the Physical Medium Dependent (PMD) function for the fiber-optic medium. Figure 1 shows a top-level 100BASE-FX connection. The connections between the PHY and the fiber-optic transceiver require external circuitry to function properly.

**Figure 1 100BASE-FX PECL/LVPECL Interface**




All Cortina 100BASE-FX products can interface with either a 5 V or 3.3 V fiber-optic transceiver. (PECL and LVPECL can be interfaced to each other with proper external circuitry). Cortina recommended circuitry is provided to interface 3.3 V and 2.5 V Cortina PHYs to both 5 V and popular 3.3 V fiber-optic transceivers. Refer to the fiber-optic manufacturer for power decoupling and termination circuit recommendations. All interface recommendations in this document are optimized for best performance.

Table 1 lists the PHYs discussed in this document.

**Table 1 100BASE-FX PHYs Discussed**

| Product | Power Supply |
|---|---|
| LXT971A | 3.3 V |
| LXT973 | 2.5 V |
| LXT9785/LXT9785E | 2.5 V |

## 1.2 ECL / PECL / LVPECL Concepts

This section describes ECL, PECL, and LVPECL concepts. PECL and LVPECL logic levels are used to interface Cortina PHYs with fiber-optic transceivers.

### 1.2.1 ECL

Emitter Coupled Logic (ECL) is a non-saturating logic family capable of high speeds with low rise and fall times. These characteristics make ECL an ideal choice for high-speed serial communications. ECL uses two supply voltages: 0 V and –5.2 V. The two logic voltage levels used for signaling are a function of the upper supply voltage (0 V in this case). The output High voltage ($V_{OH}$) is generally –0.9 ($V_{CC}$ – 0.9 V) and the output Low voltage ($V_{OL}$) is generally –1.7 V ($V_{CC}$ – 1.7 V).

### 1.2.2 PECL

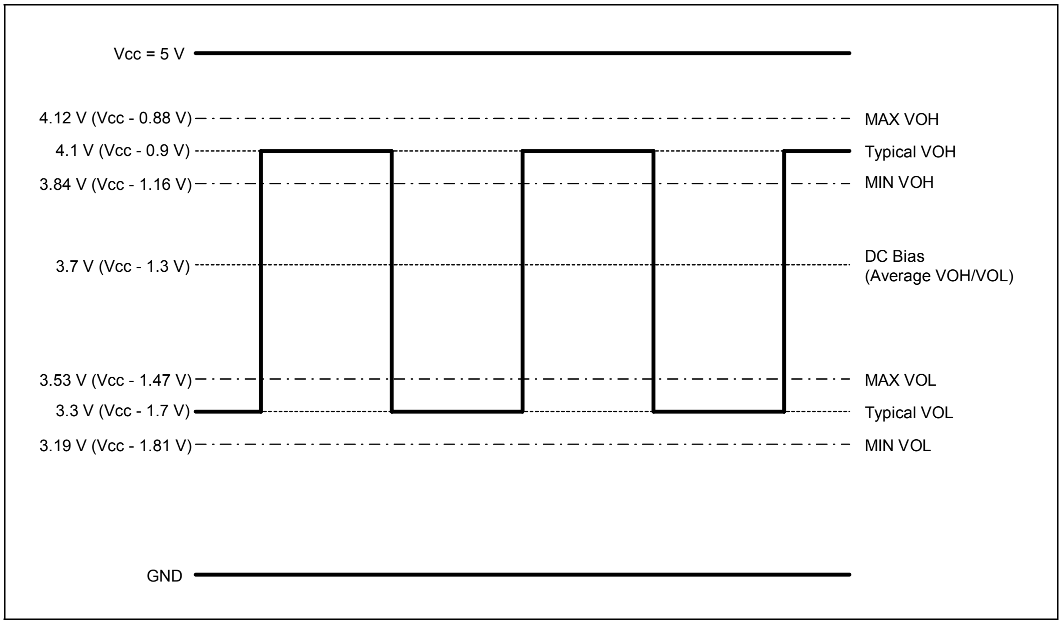
PECL is similar to ECL with a positive supply voltage. PECL operates in exactly the same manner as ECL, except that it uses a +5 V upper supply voltage and a 0 V lower supply voltage (instead of 0 V and –5.2 V). PECL offers the same non-saturating, high-speed serial communication features as ECL, as well as the same output voltage characteristics ($V_{OH} = V_{CC} – 0.9$ V and $V_{OL} = V_{CC} – 1.7$ V). The advantage of PECL (over ECL) is that its positive supply voltage provides a CMOS compatible interface. PECL interfaces provide low impedance outputs and high impedance inputs.

In PECL, $V_{OH}$ is generally 4.1 V ($V_{CC}$ – 0.9 V) and $V_{OL}$ is generally 3.3 V ($V_{CC}$ – 1.7 V). Since these voltages are dependent on $V_{CC}$, they will change as $V_{CC}$ changes.

**Note:** It is important to have a clean and constant 5 V supply voltage. Always decouple any 5 V supply voltage used on a PECL interface to minimize noise.

The average of the $V_{OH}$ and $V_{OL}$ signal levels is 3.7 V ($V_{CC}$ – 1.3 V). This 3.7 V DC bias is an important consideration when AC coupling a PECL interface, and is discussed in more detail in later sections. Figure 2 shows the signaling levels used for PECL logic.

**Figure 2 PECL Signaling**




## 1.2.3 LVPECL

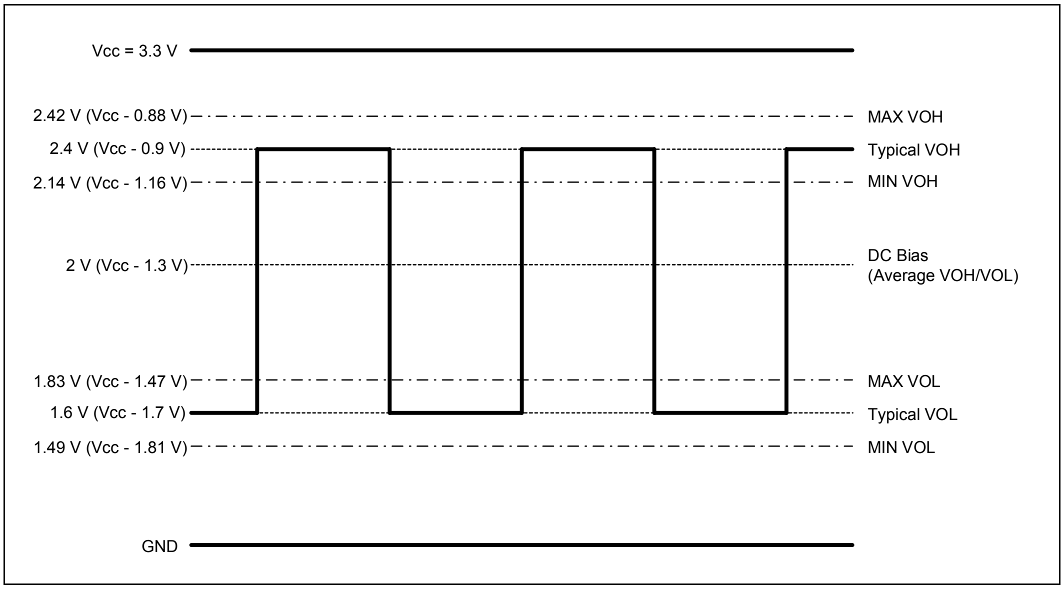
LVPECL operates in the same manner as PECL with one distinct difference: the upper supply voltage ($V_{CC}$) is 3.3 V (instead of 5 V). LVPECL offers the same non-saturating, high-speed serial communication features as ECL/PECL, and the same output voltage characteristics ($V_{OH} = V_{CC} – 0.9$ V and $V_{OL} = V_{CC} – 1.7$ V). The advantage of LVPECL (over ECL) is that its positive supply voltage provides for a CMOS compatible interface. LVPECL interfaces provide low impedance outputs and high impedance inputs.

As in ECL and PECL, the two logic voltage levels used for signaling are a function of the upper supply voltage (3.3 V in this case). $V_{OH}$ is generally 2.4 V ($V_{CC}$ – 0.9 V) and $V_{OL}$ is generally 1.6 V ($V_{CC}$ – 1.7 V). Since these voltages are dependent on $V_{CC}$, they will change as $V_{CC}$ changes.

**Note:** It is important to have a clean and constant 3.3 V supply voltage. Always decouple any 3.3 V supply voltage used on an LVPECL interface to minimize noise.

The average of the $V_{OH}$ and $V_{OL}$ signal levels is 2 V ($V_{CC}$ – 1.3 V). This 2 V DC bias is an important consideration when AC coupling an LVPECL interface, and is discussed in more detail in later sections. Figure 3 shows the signaling levels used for LVPECL logic.

**Figure 3 LVPECL Signaling**




## 1.3 Fundamental Design Considerations

This section describes the general principles used to design a standard PECL/LVPECL interface. Cortina PHYs use variations of PECL/LVPECL signaling. Some of these general principles are modified in actual interface designs to reflect these variations. Use this section to become familiar with the standard PECL/LVPECL interface. Section 2.0 and Section 3.0 provide descriptions of detailed designs using Cortina PHYs.

PECL/LVPECL 100BASE-FX interfaces have the following three distinct signals as shown in Figure 1 on page 5:

- Transmit
- Receive
- Signal Detect

The transmit side sends a differential 125 Mbaud, 5B encoded NRZI serial data stream from the PHY to the fiber transceiver for transmission onto a fiber-optic media. The NRZI stream operates at the specified PECL/LVPECL voltage levels. The receive side operates in the same manner as the transmit side in the opposite direction. Signal detect is used to indicate a valid link from the fiber-optic media. An output High PECL/LVPECL voltage on signal detect indicates to the PHY that link activity on the receive interface is valid. An output low PECL/LVPECL voltage on signal detect indicates to the PHY that invalid link conditions exist (the optical power at the fiber-optic transceiver input has fallen below a minimum threshold), and the link is disabled.

Standard PECL/LVPECL outputs require an emitter current path for the drivers to function properly. This current path is usually provided on the interface (unless the sourcing device provides this internally). Instead of providing a current path to ground on the interface, a current path to a higher voltage (below signal voltage levels) is sometimes used to reduce power consumption on the interface.

### 1.3.1 General PCB / Transmission Line Considerations

Use the following general line considerations when designing the PHY/fiber transceiver interface layout:

- Match source, transmission line, and load impedances as closely as possible to minimize losses and reflections.

**Note:** A 100 Ω differential/50 Ω single-ended characteristic impedance is assumed throughout this document. Designs may have to be modified when there are changes to this assumption.

- Eliminate PCB/transmission line discontinuities that can cause poor signal performance.
- Eliminate stubs or branches that can result in signal reflections and degradations.
- Route differential signals on the same board layer.
- Route differential signals close to each other with nothing between them.
- Match trace lengths for differential signals (positive and negative).
- Route signals with traces that are a short as possible.

### 1.3.2 Transmit and Receive Interfaces

The transmit and receive interfaces use differential PECL/LVPECL signaling. Since the serial data stream uses a NRZI format, the differential signal is purely a high-frequency AC signal (with a $V_{CC}$ – 1.3 V DC bias). This allows the differential lines to be either DC or AC coupled.

#### 1.3.2.1 DC Coupling

Cortina recommends DC coupling on all *standard* PECL-to-PECL or LVPECL-to-LVPECL interfaces.

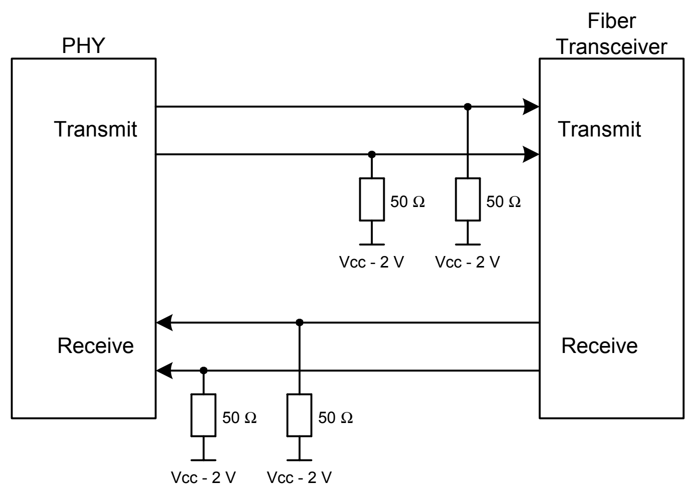
Use the following general design guidelines:

- Provide a current path to approximately $V_{CC}$ – 2 V (PECL = 3 V, LVPECL = 1.3 V).
- Provide a proper 100 Ω differential impedance termination unless internally terminated by input devices.
- Place the resistor network as close as possible to the signal input device.

Figure 4 illustrates these concepts.

**Note:** Figure 4 is intended as a conceptual tool, and is not a design recommendation.

**Figure 4 Standard PECL/LVPECL–DC Coupled Transmit and Receive Concepts**




### 1.3.2.2 AC Coupling

Cortina recommends AC coupling on all *non-standard* PECL-to-PECL or LVPECL-to-LVPECL interfaces. In addition, AC coupling is required on all LVPECL-to-PECL or PECL-to-LVPECL interfaces. When interfacing between LVPECL and PECL, AC coupling eliminates the DC bias from the output device side of the capacitors, while a resistor network on the input device side of the capacitors can re-bias the signals to the required DC level ($V_{CC}$ – 1.3 V).

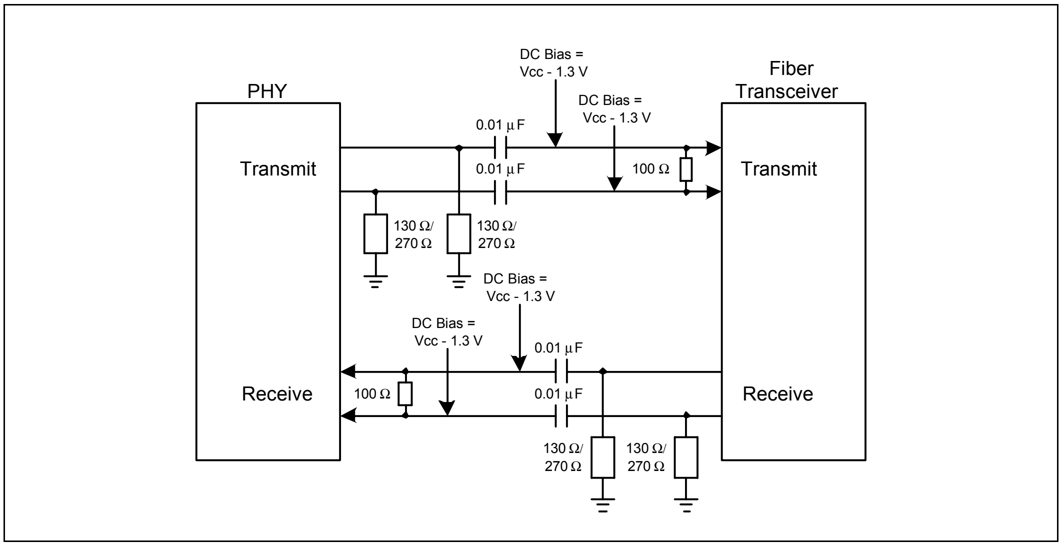
Use the following general design guidelines:

- Place 0.01 µF capacitors on the signal lines to AC couple the signal.
- Provide a current path to ground on the output device side of the capacitors.
- Provide proper DC bias circuitry of $V_{CC}$ – 1.3 V (PECL = 3.7 V, LVPECL = 2 V) with an equivalent, 100 Ω differential impedance.
- Place the bias circuitry as close to the input device as possible.

Figure 5 illustrates these concepts.

**Note:** Figure 5 is intended as a conceptual tool, and is not a design recommendation.

**Figure 5 Standard PECL/LVPECL–AC Coupled Transmit and Receive Concepts**




### 1.3.3 Signal Detect SD Interface

SD uses a single-ended PECL/LVPECL interface, and is effectively a DC signal (minimal $V_{OH}/V_{OL}$ switching). Therefore, the signal detect line must be DC coupled.

#### 1.3.3.1 DC Coupling

DC coupling is recommended on all standard PECL-to-PECL or LVPECL-to-LVPECL interfaces. Special circuitry is required for the PECL-to-LVPECL or LVPECL-to-PECL interfaces to function properly, and is described in Section 2.0 and Section 3.0.

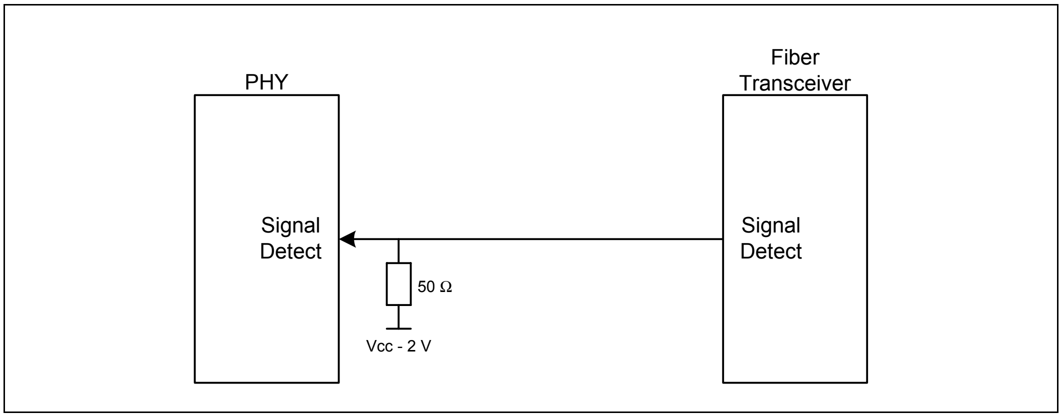
Use the following general design guideline:

- Provide a current path to approximately $V_{CC}$ – 2 V(PECL = 3 V, LVPECL = 1.3 V) with a 50 Ω equivalent impedance.

Figure 6 illustrates this concept.

**Note:** Figure 6 is intended as a conceptual tool, and is not a design recommendation.

**Figure 6 Standard PECL / LVPECL–Signal Detect Concepts**



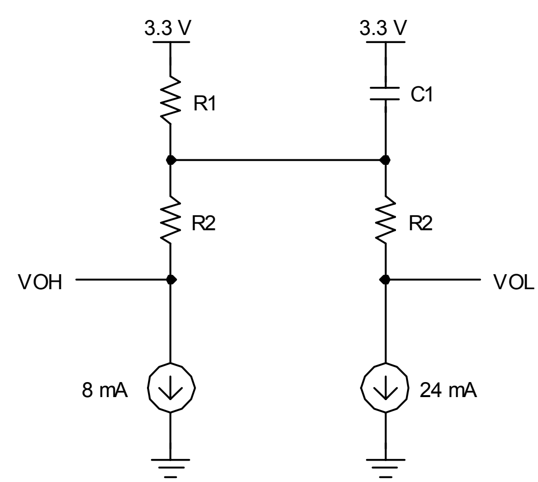
# 2.0 3.3 V Physical Layer Devices

## 2.1 General Description

The Cortina Systems® LXT971A is a 3.3 V Physical Layer device that provides an LVPECL interface for connection to an external Fast Ethernet fiber-optic transceiver. The device can interface to 3.3 V and 5 V fiber-optic transceivers.

Cortina 3.3 V PHY transmitter outputs (TPFOP/N) behave as current sources. The current draw is 24 mA for logic Low outputs, and 8 mA for logic High outputs. Figure 7 models the behavior of the output stage. Since the output is differential, there is a constant 32 mA flowing through resistor R1. The capacitor (C1) provides any switching current resulting from imperfect matching of the output current sources. The resistor values R1 and R2 should be chosen to provide correct LVPECL $V_{OL}$ and $V_{OH}$ voltage levels. The recommended values for R1 and R2 are 16 Ω and 50 Ω, respectively.

**Figure 7 3.3V PHY Transmit LVPECL Characteristics**




The receiver inputs of Cortina 3.3 V devices require standard LVPECL signal levels. The input pair (TPFIP/N) does not contain internal termination. An external network on the input pair (TPFIP/N) interface is necessary to achieve the required 100 Ω differential termination. For good noise rejection, a minimum differential input signal swing of at least 500 mV is recommended.

## 2.2 Interfacing a 5 V Fiber-Optic Transceiver

The following sub-sections and diagrams provide decoupling, biasing, and termination information essential for a successful fiber connection using Cortina 3.3 V devices and 5 V fiber-optic transceivers. The recommended 5 V fiber-optic transceiver in this application is the Agilent Technologies* HFBR-5103. The HFBR-5103 uses standard PECL signaling on all inputs and outputs.

### 2.2.1 Transmit Interface Circuitry

Cortina 3.3 V devices need to be AC coupled to the HFBR-5103 using a 0.01 µF capacitor to convert LVPECL signals to PECL signals on the transmit pair. The 16 Ω/50 Ω combination on the PHY side of the capacitors sets the proper LVPECL voltages from the current levels as shown in Figure 9. The 0.01 µF capacitors eliminate the 2 V LVPECL bias. The 1.1 kΩ (1.15 kΩ)/3.1 kΩ combination shown in Figure 9 provides a 3.7 V PECL bias and a 40 mV differential offset voltage (see Appendix A, *Crosstalk Amplification*) to the fiber transceiver input. (The relatively large resistor values in parallel with the 50 Ω resistors on the PHY side of the AC coupling capacitors keep the equivalent single-ended termination close to 50 Ω.)

### 2.2.2 Receive Interface Circuitry

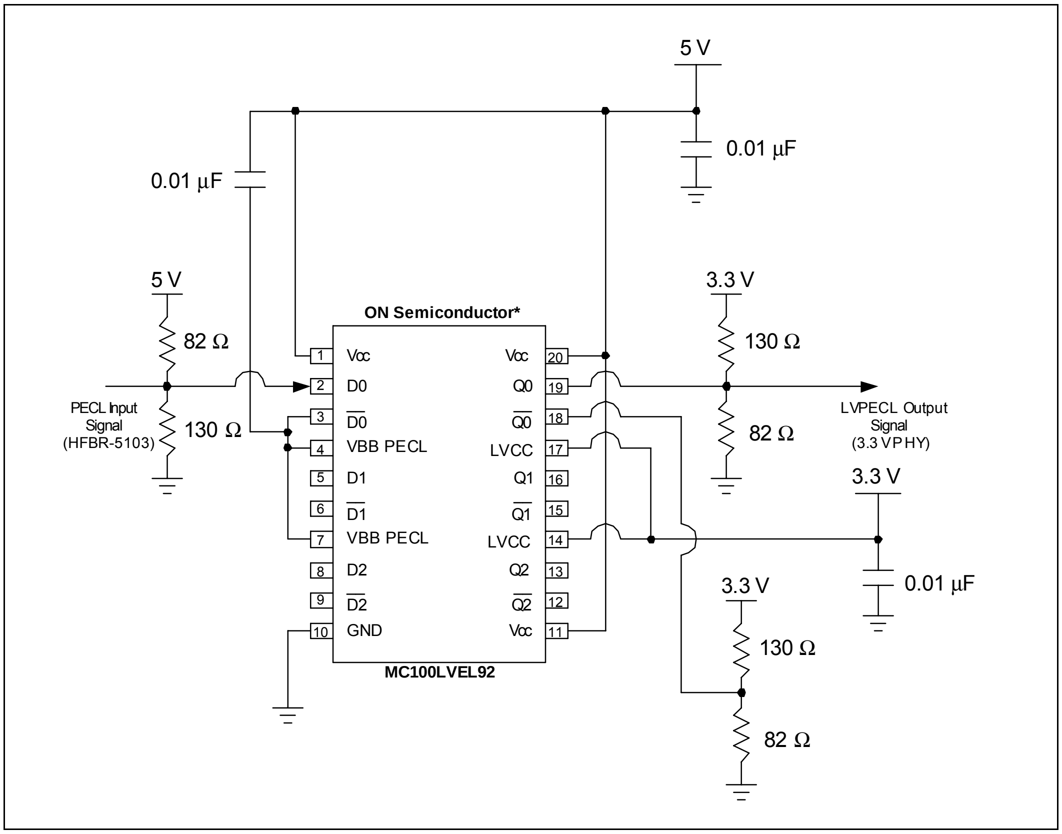
Cortina 3.3 V devices use LVPECL signal levels on their receive inputs. AC coupling is necessary to convert the HFBR-5103 standard PECL outputs to the LVPECL input levels. The 270 Ω resistors to ground in Figure 9 provide the necessary emitter current path for the output pair of the fiber transceiver. The 0.01 µF AC coupling capacitors remove the PECL DC bias from the signal. The 102 Ω/154 Ω resistor combination provides a 2 V bias for the LVPECL input. (The 102 Ω/154 Ω resister values in parallel with the 270 Ω resistors on the fiber transceiver side of the AC coupling capacitors create an equivalent single-ended termination of approximately 50 Ω.)

### 2.2.3 Signal Detect Interface Circuitry

The SD pin identifies remote fault conditions on the line. The LXT971A supports the signal detect function.

The HFBR-5103 provides a standard PECL signal detect output. The signal detect pin on Cortina 3.3 V PHYs requires a standard LVPECL input. Since the interface must be DC coupled (see Section 1.3.2, *Transmit and Receive Interfaces*, on page 9), a conversion from the HFBR-5103 PECL output to the LVPECL input is required. This cannot be done with passive components because the ratio conversions of the PECL signal will not meet the voltage thresholds of LVPECL. A PECL-to-LVPECL logic translator is required for this conversion. Figure 8 shows the ON Semiconductor* MC100LVEL92 triple PECL-to-LVPECL logic translator and required interface circuitry for this device. The resistor combinations provide 50 Ω emitter current paths to VCC – 2 V. The logic translator allows for up to three SD interfaces (ports) per device. Refer to the ON Semiconductor* MC100LVEL92 datasheet for component specifications.

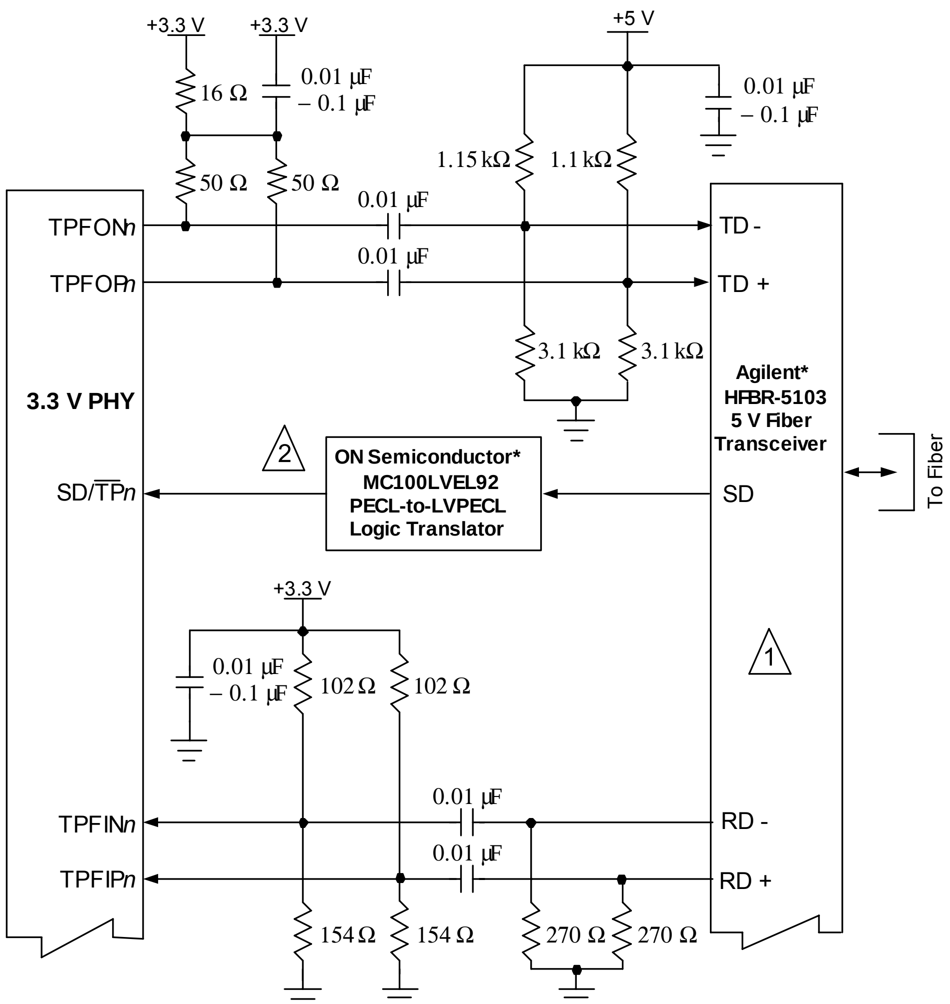
**Figure 8 ON Semiconductor* Triple PECL-to-LVPECL Translator**




## 2.2.4 Design Recommendation

Figure 9 shows the recommended interface circuitry for an Cortina 3.3 V PHY and the Agilent* HFBR-5103 5 V fiber-optic transceiver.

**Figure 9 Recommended 3.3 V PHY-to-5 V Fiber Transceiver Interface Circuitry**




1. Refer to the transceiver manufacturers recommendations for termination circuitry.
2. See Figure 8 for recommended logic translator circuitry.

## 2.3 Interfacing a 3.3 V Fiber-Optic Transceiver

The following sub-sections and diagrams provide decoupling, biasing, and termination information essential for a successful fiber connection using Cortina 3.3 V devices and 3.3 V fiber-optic transceivers. The recommended 3.3 V fiber-optic transceiver in this application is the Agilent Technologies* HFBR-5903. The HFBR-5903 uses standard LVPECL signaling on all inputs and outputs.

### 2.3.1 Transmit Interface Circuitry

Cortina 3.3 V devices can be DC coupled to the HFBR-5903 and other standard LVPECL fiber-optic transceivers that do not terminate the transmit pair internally. The 16 Ω/50 Ω resistor combination shown in Figure 10 sets the proper LVPECL voltages from the current levels, and provides an equivalent load impedance of 50 Ω. The 2.74 kΩ pull-down resistor, combined with the internal power-down, loopback, and reset transmitter characteristics of Cortina 3.3 V PHYs, provides a 60 mV differential offset voltage in these states (see Appendix A, *Crosstalk Amplification*), while not impacting the interface during normal operation.

### 2.3.2 Receive Interface Circuitry

Cortina 3.3 V devices use standard LVPECL signal levels on their receive inputs. DC coupling can be used with the HFBR-5903. The 130 Ω/82 Ω resistor combination shown in Figure 10 provides an equivalent load impedance of 50 Ω, and an emitter current path to 1.3 V.

### 2.3.3 Signal Detect Interface Circuitry

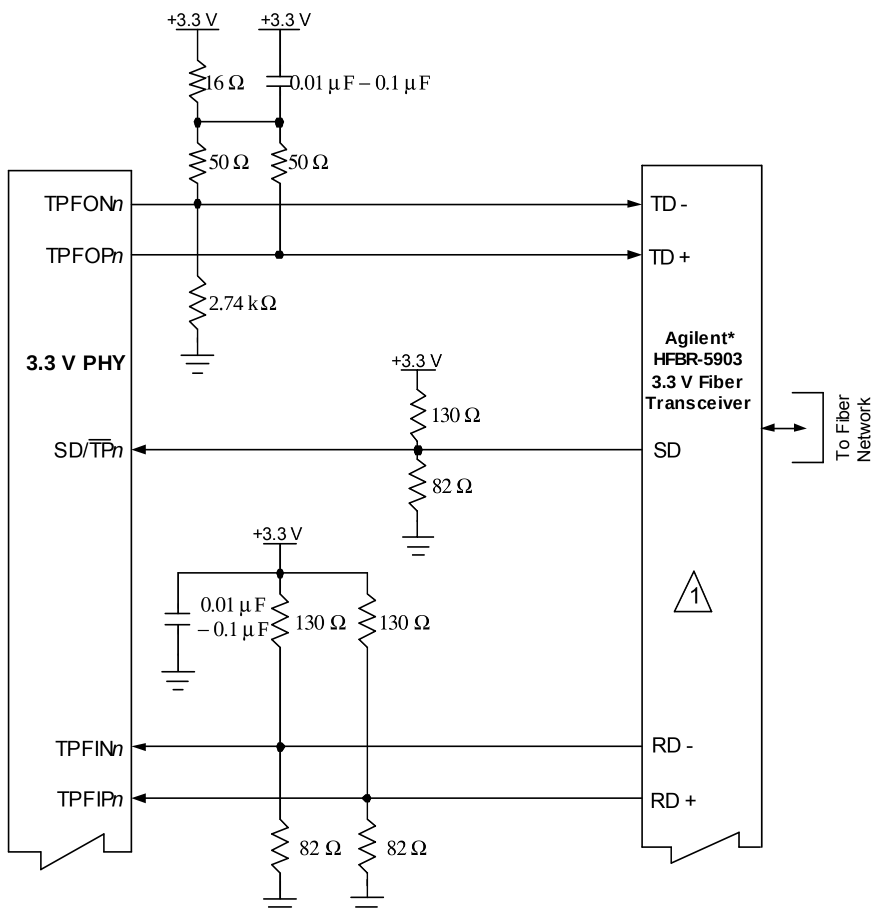
The SD pin identifies remote fault conditions on the line. The LXT971A supports the signal detect function.

The HFBR-5903 provides a standard LVPECL signal detect output. The 130 Ω/82 Ω resistor combination shown in Figure 10 provides an equivalent load impedance of 50 Ω, and an emitter current path to 1.3 V.

### 2.3.4 Design Recommendation

Figure 10 shows the recommended interface circuitry for an Cortina 3.3 V PHY and the Agilent* HFBR-5903 3.3 V fiber-optic transceiver.

## Figure 10 Recommended 3.3 V PHY-to-3.3 V Fiber Transceiver Interface Circuitry




1. Refer to the transceiver manufacturers' recommendations for termination circuitry.

# 3.0 2.5 V Physical Layer Devices

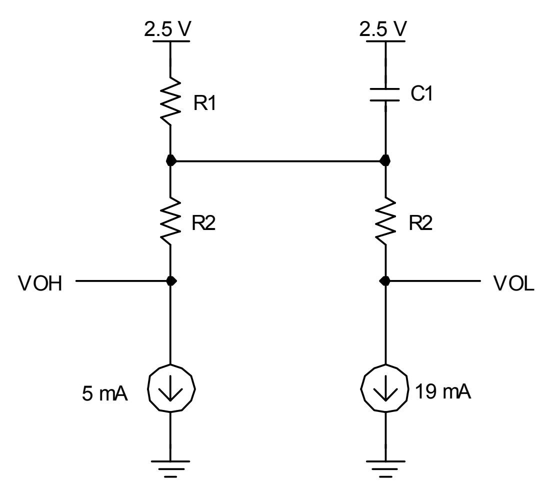
## 3.1 General Description

The Cortina Systems® LXT973 and Cortina Systems® LXT9785/9785E are 2.5 V Physical Layer devices that provide an LVPECL interface for connection to an external Fast Ethernet fiber-optic transceiver. They can be interfaced to 3.3 V and 5 V fiber-optic transceivers.

Cortina 2.5 V PHY transmitter outputs (TPFOP/N) behave as current sources. The current draw is 19 mA for logic Low outputs, and 5 mA for logic High outputs. Figure 11 models the behavior of the output stage. Since the output is differential, there is a constant 24 mA flowing through resistor R1. The capacitor (C1) provides any switching current resulting from imperfect matching of the output current sources.

In power-down, power-up, and reset modes, the transmitter outputs are pulled to the supply voltage used in Figure 11. In applications where the power-down feature is used during normal operations, the supply voltage must not exceed 3 V to avoid damaging the output stage. To eliminate this concern, a 2.5 V supply is used and the transmit interface is AC coupled and re-biased to meet the fiber transceiver input levels. The resistor values R1 and R2 are chosen to generate a 700 mV differential between $V_{OL}$ and $V_{OH}$. The minimum output voltage of the transmitter should stay above 600 mV to avoid output distortion. This limits the R1-R2 network to a minimum supply voltage of about 2.2 V. The recommended values for R1 and R2 are 27 Ω and 50 Ω, respectively.

**Figure 11 2.5 V PHY Transmit LVPECL Characteristics**




Cortina 2.5 V PHY receiver inputs (TPFIP/N) typically fall between ground and 2.5 V, and must not exceed the 2.5 V supply by more than 500 mV. LVPECL (3.3 V) fiber modules are acceptable ($V_{OH}$ = 3.3 V – 0.88 V = 2.42 V). The situation is still acceptable if the 3.3 V fiber module supply is 5% high and the 2.5 V supply is 5% low. If input signals are used that peak above the 2.5 V supply voltage, AC coupling capacitors are needed. Resistive dividers on the PHY side of the capacitors can be used to set the common mode

voltage halfway between the 2.5 V supply and ground. Cortina recommends a minimum differential input signal swing of greater than 500 mV for good noise rejection. The inputs contain a 100 Ω internal termination (differential).

## 3.2 Interfacing a 5 V Fiber-Optic Transceiver

The following sub-sections and diagrams provide decoupling, biasing, and termination information essential for a successful fiber connection using Cortina 2.5 V devices and 5 V fiber-optic transceivers. The recommended 5 V fiber-optic transceiver in this application is the Agilent* HFBR-5103. The HFBR-5103 uses standard PECL signaling on all inputs and outputs.

### 3.2.1 Transmit Interface Circuitry

Cortina 2.5 V devices need to be AC coupled to the HFBR-5103 using a 0.01 µF capacitor to convert the PHY output signals to PECL signals on the transmit pair. The 27 Ω/50 Ω combination on the PHY side of the capacitors sets the proper 700 mV differential voltage with a 1.25 V bias from the current levels as shown in Figure 13. The 0.01 µF capacitors eliminate the 1.25 V bias. The 1.1 kΩ (1.15 kΩ)/3.1 kΩ combination shown in Figure 13 provides a 3.7 V PECL bias and a 40 mV differential offset voltage (see Appendix A, *Crosstalk Amplification*) to the fiber transceiver input. (The relatively large resistor values in parallel with the 50 Ω resistors on the PHY side of the AC coupling capacitors keep the equivalent single-ended termination close to 50 Ω.)

### 3.2.2 Receive Interface Circuitry

Cortina 2.5 V devices are tolerant to signals with bias levels of between 1 V and 2.5 V (with a 600 mV – 800 mV differential) on their receive inputs. AC coupling is necessary to convert the HFBR-5103 standard PECL outputs (3.7 V bias) to input levels with a bias level of between 1 V and 2.5 V. The 270 Ω resistors to ground in Figure 13 provide the necessary emitter current path for the output pair of the fiber transceiver. The 0.01 µF AC coupling capacitors remove the PECL DC bias from the signal. The 127 Ω/118 Ω resistor combination provides a 1.2 V bias for the receive input. (The127 Ω/118 Ω resister values in parallel with the 270 Ω resistors on the fiber transceiver side of the AC coupling capacitors create an equivalent single-ended termination of approximately 50 Ω.)

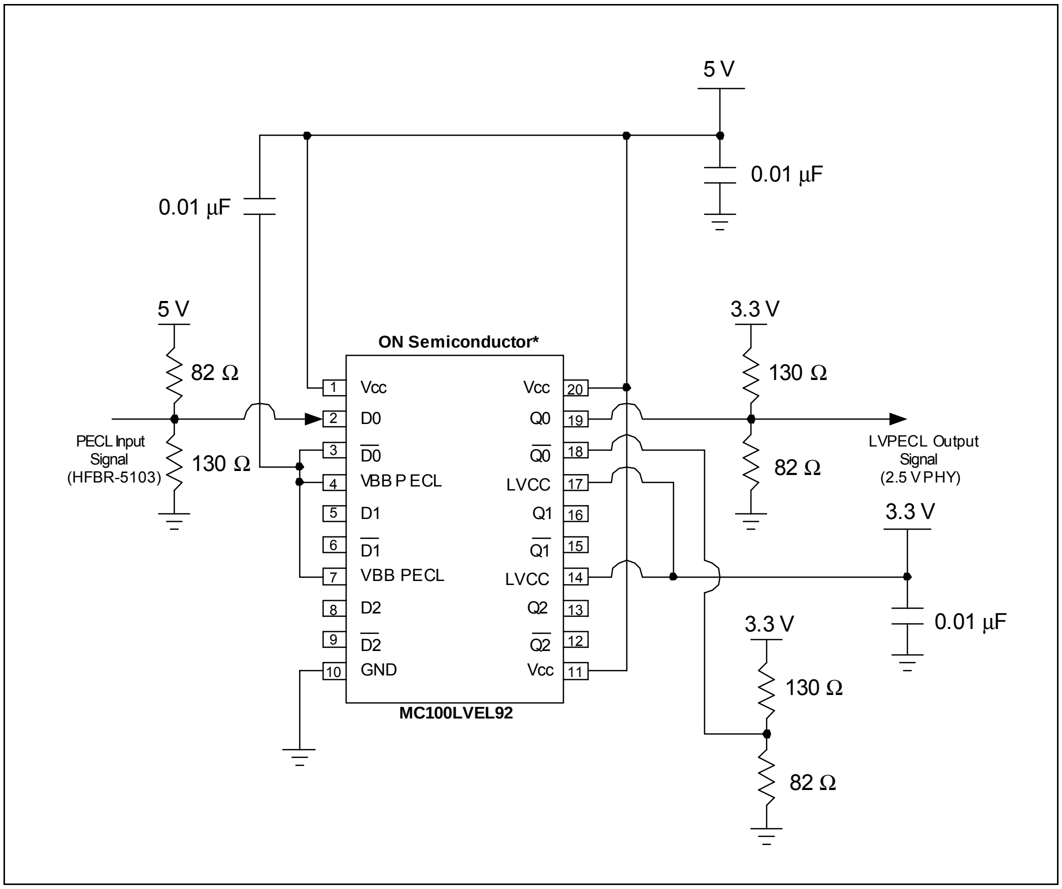
### 3.2.3 Signal Detect Interface Circuitry

The SD pin identifies remote fault conditions on the line. The LXT9785(E) and LXT973 support the signal detect function.

**Note:** Cortina 2.5 V devices have a feature that allows the Signal Detect pin to use 3.3 V as a reference supply voltage or 2.5 V as a reference supply voltage (internally). The LXT9785/9785E and LXT973 Datasheets (document numbers 249241 and 249426) explain this feature in more detail. This application note assumes a 3.3 V reference supply voltage (VCCPECL = 3.3 V) to allow for standard LVPECL inputs.

The Agilent* HFBR-5103 provides a standard PECL signal detect output. The signal detect pin on Cortina 2.5 V PHYs requires a standard LVPECL input. Since the interface must be DC coupled (see Section 1.3.2, *Transmit and Receive Interfaces*, on page 9), a logic conversion from the HFBR-5103 PECL output to the LVPECL input is required. This cannot be done with passive components because the ratio conversions of the PECL signal do not meet the voltage thresholds of LVPECL. A PECL-to-LVPECL logic translator is required for this conversion. Figure 12 shows the ON Semiconductor* MC100LVEL92 triple PECL-to-LVPECL logic translator and required interface circuitry for this device. The resistor combinations provide 50 Ω emitter current paths to VCC – 2 V. The logic translator allows for up to three SD interfaces (ports) per device. Refer to the MC100LVEL92 Datasheet for component specifications.

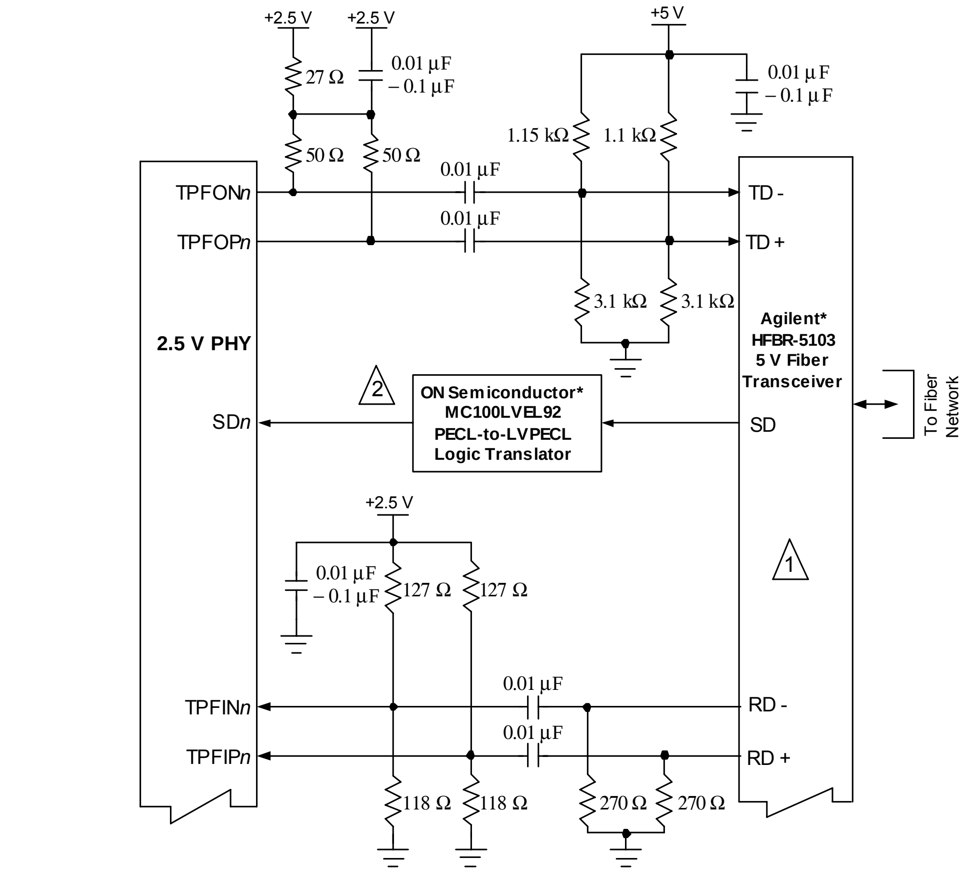
**Figure 12 ON Semiconductor* Triple PECL-to-LVPECL Translator**




## 3.2.4 Design Recommendation

Figure 13 shows the recommended interface circuitry for an Cortina 2.5 V PHY and the Agilent* HFBR-5103 5 V fiber-optic transceiver.

**Figure 13 Recommended 2.5 V PHY-to-5 V Fiber Transceiver Interface Circuitry**




1. Refer to the transceiver manufacturers' recommendations for termination circuitry.
2. See Figure 12 for recommended logic translator circuitry.

## 3.3 Interfacing a 3.3 V Fiber-Optic Transceiver

The following sub-sections and diagrams provide decoupling, biasing, and termination information essential for a successful fiber connection using Cortina 2.5 V devices and 3.3 V fiber-optic transceivers. The recommended 3.3 V fiber-optic transceiver in this application is the Agilent* HFBR-5903. The HFBR-5903 uses standard LVPECL signaling on all inputs and outputs.

### 3.3.1 Transmit Interface Circuitry

Cortina 2.5 V devices need to be AC coupled to the HFBR-5903 using a 0.01 µF capacitor to convert the PHY output signals to LVPECL signals on the transmit pair. The 27 Ω/50 Ω combination on the PHY side of the capacitors sets the proper 700 mV differential voltage with a 1.25 V bias from the current levels as shown in Figure 14. The 0.01 µF capacitors eliminate the 1.25 V bias. The 1.3 kΩ (1.4 k Ω)/2 kΩ combination shown in Figure 14 provides a 2 V LVPECL bias and a 60 mV differential offset voltage (see Appendix A, *Crosstalk Amplification*) to the fiber transceiver input. (The relatively large resistor values in parallel with the 50 Ω resistors on the PHY side of the AC coupling capacitors keep the equivalent single-ended termination close to 50 Ω.)

### 3.3.2 Receive Interface Circuitry

Cortina 2.5 V devices are tolerant to signals with bias levels of between 1 V and 2.5 V (with a 600 mV – 800 mV differential) on their receive inputs. Since LVPECL uses a 2 V bias, Cortina 2.5 V devices can use standard LVPECL signal levels on their receive inputs. DC coupling can be used with the HFBR-5903. The 130 Ω resistors to ground in Figure 14 provide the necessary emitter current path for the output pair of the fiber transceiver. The 100 Ω termination on the receive side is built into the Cortina 2.5 V devices and is not required externally. All components (on the transmit and receive side) should be placed close to the fiber transceiver.

### 3.3.3 Signal Detect Interface Circuitry

The SD pin identifies remote fault conditions on the line. The LXT9785/9785E and LXT973 transceivers support the signal detect function.

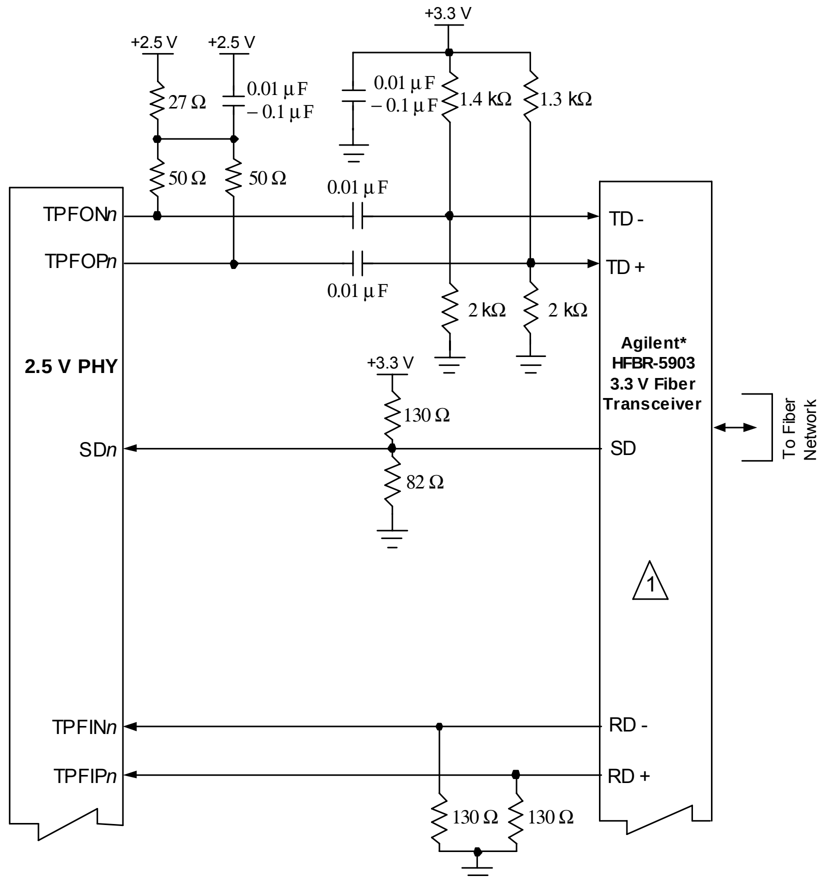
**Note:** Cortina 2.5 V devices have a feature that allows the signal detect pin to use 3.3 V as a reference supply voltage or 2.5 V as a reference supply voltage (internally). The LXT9785/9785E and LXT973 Datasheets explain this feature in more detail. This application note assumes a 3.3 V reference supply voltage (VCCPECL = 3.3 V) to allow for standard LVPECL inputs.

The HFBR-5903 provides a standard LVPECL signal detect output. The 130 Ω/82 Ω resistor combination shown in Figure 14 provides an equivalent load impedance of 50 Ω, and an emitter current path to 1.3 V.

### 3.3.4 Design Recommendation

Figure 14 shows the recommended interface circuitry for an Cortina 2.5 V PHY and the Agilent* HFBR-5903 3.3 V fiber-optic transceiver.

## Figure 14 Recommended 2.5 V PHY-to-3.3 V Fiber Transceiver Interface Circuitry




1. Refer to the transceiver manufacturers' recommendations for termination circuitry.

# 4.0 Reference Material

## 4.1 100BASE-FX Product Index

Table 2 shows a list of the recommended Cortina Physical Layer products that support 100BASE-FX operation. The recommended interface circuitry with 3.3 V and 5 V fiber-optic applications for each product is referenced. The Datasheet and Design and Layout Guide for the selected product should be used with this document for 100BASE-FX designs.

**Table 2 PHYs Supporting 100BASE-FX Operation**

| Product | Power Supply | Interface | 5 V Fiber-Optic Transceiver Interface Circuitry | 3.3 V Fiber-Optic Transceiver Interface Circuitry |
|---|---|---|---|---|
| LXT971A | 3.3 V | LVPECL | Figure 8 on page 15 and Figure 9 on page 16 | Figure 10 on page 18 |
| LXT973 | 2.5 V | LVPECL | Figure 12 on page 21 and Figure 13 on page 22 | Figure 14 on page 24 |
| LXT9785/ LXT9785E | 2.5 V | LVPECL | Figure 12 on page 21 and Figure 13 on page 22 | Figure 14 on page 24 |

## 4.2 100BASE-FX Fiber-Optic Transceiver Vendors

Table 3 shows a list of 1300 nm 100BASE-FX transceiver products. The Agilent Technologies* products have been validated by Cortina with the interface recommendations in this application note. The other products have not been validated by Cortina.

**Note:** The list of 100BASE-FX fiber optic transceiver vendors in Table 3 is for reference only and does not constitute a recommendation by Cortina for these vendors or their products.

**Table 3 100BASE-FX Fiber Optic Transceiver Vendors**

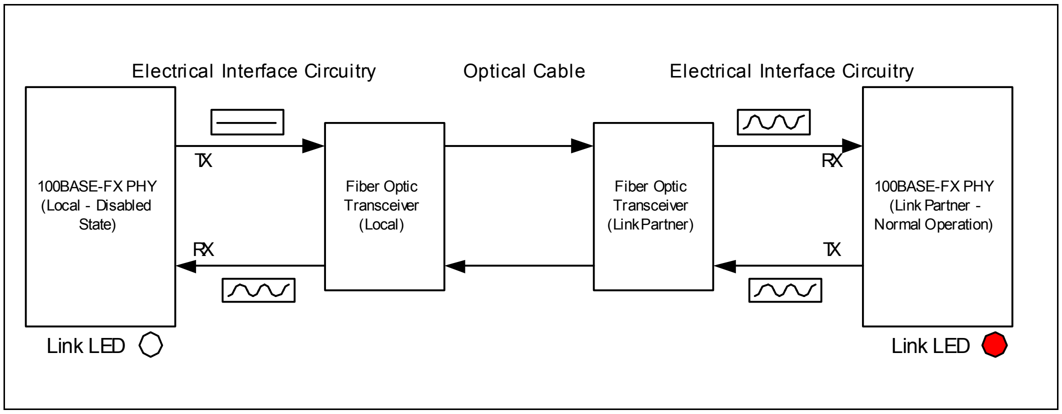
| Vendor | 5 V Fiber Transceiver | 3.3 V Fiber Transceiver | Company Web Site |
|---|---|---|---|
| Agilent Technologies* | HFBR-5103 | HFBR-5903 | www.agilent.com |
| AMP* (Tyco Electronics) | — | 269147-2[1] | www.amp.com |
| Delta Electronics* | OPT-155A1H1[1] OP | T-155A2H1[1] | www.deltaww.com |
| Luminent* (MRV Communications) | 3LD9-CX[1] | 3LV9CX[1] | www.luminentinc.com |
| Infineon Technologies* (Siemens) | V23809-C8-C10[1] | V23809-C8-C10[1] | www.infineon.com |

1. These transceivers have not been tested or verified by Cortina for proper functionality with Cortina Physical Layer products.

# Appendix A Crosstalk Amplification

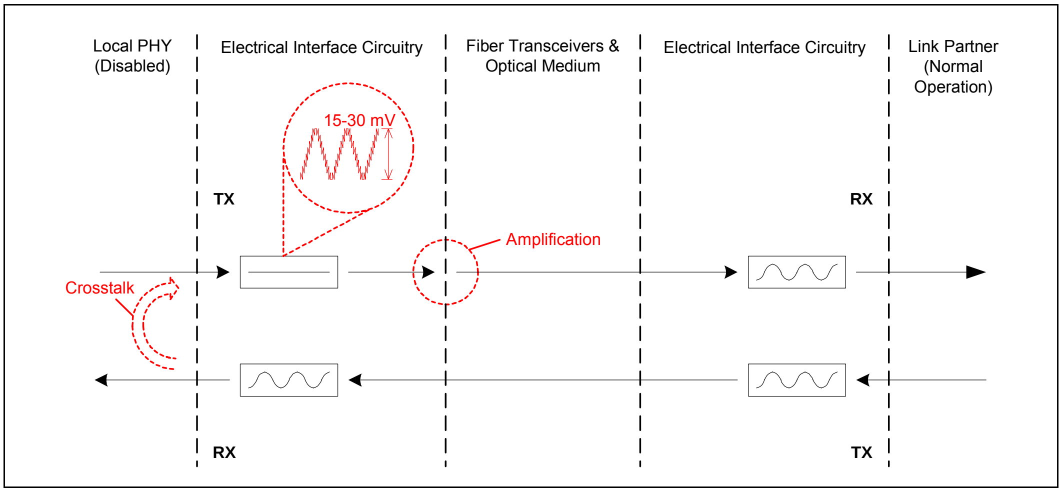
Small amounts of coupling and crosstalk are common in semiconductor devices. Many fiber optic transceivers that are designed for 100BASE-FX applications have high gains and display high sensitivities to noise on their PECL/LVPECL receivers (TX path). In a 100BASE-FX environment, these two factors can cause a condition where a remote device (link partner) in normal operating mode can perceive valid idle signals and establish link with a local device that is in a disabled state (such as power-down mode, loopback mode, or reset). Figure 15 illustrates this condition.

**Figure 15 Remote PHY Establishing Link in a Non-Valid Link Environment**




The condition in Figure 15 occurs because the link partner is in normal operating mode and is continuously transmitting idle signals. At the local device, the transmitter is disabled. However, the received idle stream from the link partner couples onto the transmit pair within the semiconductor device and produces differential noise (typically 15-30 mV peak-to-peak) that resembles an idle stream. The optical transceiver in this case is sensitive enough to detect this signal and amplify it. The link partner will then observe idle signals on its receive pair and detect that there is a valid link environment. Figure 16 shows this looped environment in more detail.

**Figure 16 Crosstalk / Amplification Condition**

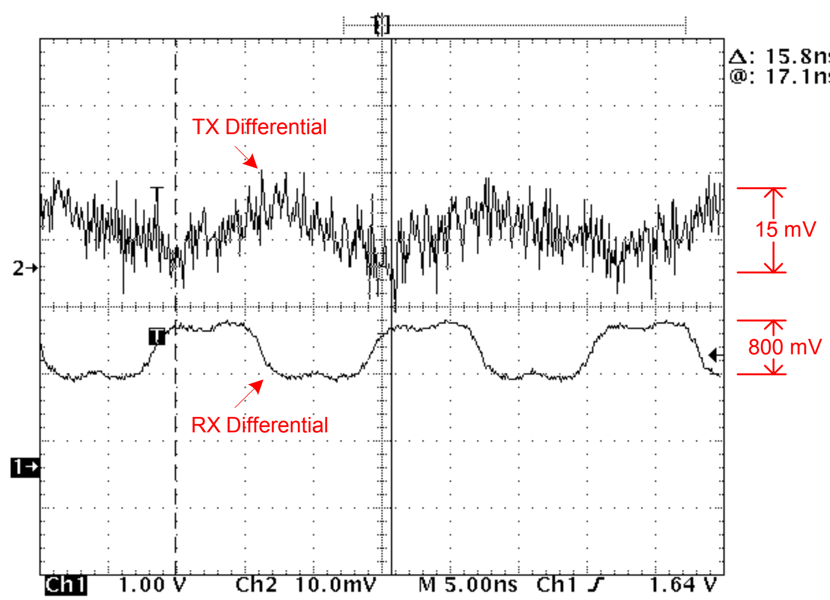


Cortina 100BASE-FX PHYs have three states where the interface enters a disabled state:

- Power-Down Mode (Hardware or Software)
- Loopback Mode (Register bit 0.14 = 1)
- Reset (Hardware or Software)

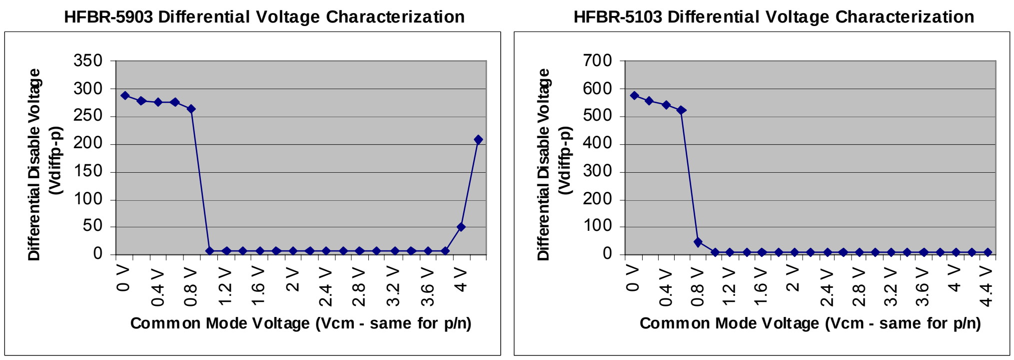
In any of these states, the transmitters of the fiber TX pair will be disabled. In a transmitter disabled state, the amount of crosstalk induced from a normal LVPECL signal (RX pair) onto the TX pair is typically 15-30 mV (peak-to-peak differential). This coupling occurs within the semiconductor device. Figure 17 shows the crosstalk seen within this environment.

**Figure 17 Semiconductor Crosstalk**



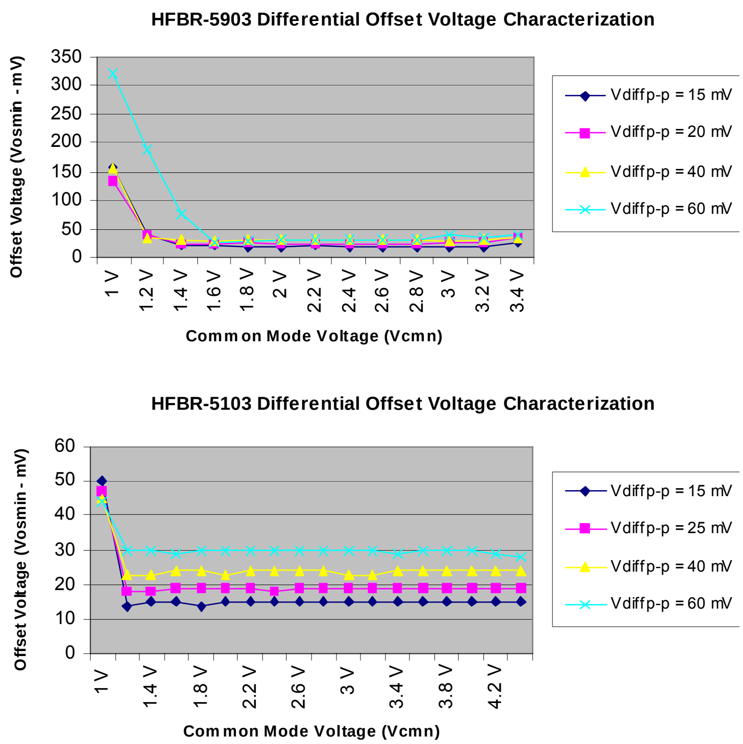

The recommended fiber optic transceivers in this document, the HFBR-5903 and the HFBR-5103, show full amplification characteristics to signals with peak-to-peak differential voltages of less than 10 mV when the common mode voltage on the TX pair is between 1.2 V and VCC (3.3 V for the HFBR-5903 and 5 V for the HFBR-5103). Figure 18 shows these performance characteristics.

**Figure 18 Fiber Transceiver Differential Voltage Thresholds for Full Amplification**




The recommended method of preventing the amplification of semiconductor crosstalk in a 100BASE-FX environment is to create a differential offset (VOS) voltage between the positive and negative lines of the transmit pair. This offset voltage can be achieved by designing it into the interface circuitry. Figure 19 shows the offset voltages (VOSmin) necessary to prevent full amplification in the HFBR-5903 and HFBR-5103 transceivers at various differential voltages. Figure 19 shows that within the 1.2 V to VCC region, VOSmin directly relates to Vdiffp-p. Further testing has shown that VOSmin is negligibly affected over 0-70oC temperature variations.

**Figure 19 Fiber Transceiver Differential Offset Voltage Thresholds**




Design targets for $V_{OS}$ are created by measuring the worst-case peak-to-peak differential crosstalk voltage in each interface recommendation, matching that value with the correct $V_{OSmin}$ in Figure 19, and multiplying that value by two to guard-band against variations. As interface circuitry is developed to meet the $V_{OS}$ design targets, further testing must be performed to ensure that the interface performance is not impacted during normal operation of the device. Table 4 on page 29 shows the $V_{OS}$ design targets for all recommended interfaces in this document.

**Table 4 $V_{OS}$ Design Targets for Recommended Interface Circuitry**

| Cortina PHY | Agilent Transceiver | Worst Case Crosstalk ($V_{diffp-p}$) | Offset Voltage Minimum ($V_{OSmin}$) | Offset Voltage Design Target ($V_{OS}$) |
|---|---|---|---|---|
| 3.3 V | HFBR-5103 (5 V) | 26 mV | 20 mV | 40 mV |
| 3.3 V | HFBR-5903 (3.3 V) | 34 mV | 30 mV | 60 mV |
| 2.5 V | HFBR-5103 (5 V) | 28 mV | 20 mV | 40 mV |
| 2.5 V | HFBR-5903 (3.3 V) | 16 mV | 30 mV | 60 mV |

**For additional product and ordering information:**

**www.cortina-systems.com**

~ End of Document ~