



# Cortina Systems® IXF1010 and IXF1110 Media Access Controller Initialization Guidelines

Application Note

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## Revision History

<b>Revision 3.0</b> <b>Revision Date: 21 March 2007</b>
First release of this document from Cortina Systems, Inc.
<b>Revision 002</b> <b>Revision Date: 03 February 2005</b>
<ul style="list-style-type: none"><li>• Modified language in CALENDAR_M under <a href="#">Section 2.4.6.1</a>.</li><li>• Removed CALENDAR_M from second bulleted list under <a href="#">Section 3.1.4</a>.</li></ul>
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Initial release.

## 1.0 Introduction

The Cortina Systems® IXF1010 and IXF1110 Media Access Controllers (IXF1010/IXF1110 MAC) are 10-port Gigabit Ethernet MAC devices. The IXF1110 MAC operates at 1000 Mbps full-duplex and provides an integrated SerDes for direct connection to fiber-optic modules. The IXF1010 MAC provides an RGMII interface and operates at 100 Mbps or 1000 Mbps full-duplex. Both devices have a SPI4-2 interface for 10 Gigabit data transfer to a Network Processor or SPI4-2 ASIC.

This document describes the sequence for system developers to use while bringing up the IXF1010/IXF1110 MAC in a system. The following sections are discussed in this document:

- [Section 2.0, Device Initialization, on page 5](#)
  - [Section 2.1, Power Supply Sequencing, on page 5](#)
  - [Section 2.2, Bring-Up Sequence, on page 5](#)
  - [Section 2.3, Default State of the Device, on page 6](#)
  - [Section 2.4, Device Configuration Registers, on page 7](#)
- [Section 3.0, Guidelines for Configuration Changes, on page 13](#)
  - [Section 3.1, Top Level Configurations, on page 13](#)
- [Section 4.0, Initialization Summary, on page 15](#)

Cortina Systems, Inc. (Cortina) recommends that the reader have sufficient knowledge of the IXF1010 MAC and IXF1110 MAC operation and register maps (found in the Cortina Systems® IXF1010 10-Port 100/1000 Mbps Ethernet Media Access Controller Datasheet and the Cortina Systems® IXF1110 10-Port Gigabit Ethernet Media Access Controller Datasheet [document numbers 249839 and 250210]).

## 1.1 Key Terms

[Table 1](#) describes the key terms used in this document.

**Table 1** Key Terms

Term	Description
AN	Auto-Negotiation
CRC	Cyclic Redundancy Check
FIFO	First In First Out Memory
MAC	Media Access Controller
PLL	Phase Locked Loop
SerDes	Serializer/Deserializer
SPI4-2	System Packet Interface Level 4 Phase 2 specification

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## 2.0 Device Initialization

This section describes the items system designers must follow when designing the IXF1010/IXF1110 MAC initialization sequence. This includes power-up sequence and hard reset requirements. The device default state is explained and the registers for changing the default configuration are listed and explained.

### 2.1 Power Supply Sequencing

Cortina recommends that the power-up and power-down sequence described in [Section 2.1.1](#) and [Section 2.1.2](#) be followed to ensure correct IXF1010/IXF1110 MAC operation. The sequence covers all IXF1010/IXF1110 MAC digital and analog supplies.

The IXF1010/IXF1110 MAC Datasheets provide detailed information on power sequencing.

**Caution:** Failure to follow the power-up and power-down sequences will damage the IXF1010/IXF1110 MAC.

#### 2.1.1 Power-Up Sequence

Ensure that the 1.8 V supplies (VDD/AVDD) are applied and stable prior to the application of the 2.5 V supplies (VDD2/AVDD2).

**Caution:** If the 2.5 V supplies (VDD2/AVDD2) exceed the 1.8 V (VDD/AVDD) supplies by more than 2.0 V during power-up, damage can occur to the ESD structures within the analog I/Os.

#### 2.1.2 Power-Down Sequence

Ensure that the 2.5 V supplies (VDD2/AVDD2) are removed prior to the removal of the 1.8 V supplies (VDD/AVDD).

**Caution:** If the 2.5 V supplies (VDD2/AVDD2) exceed the 1.8 V (VDD/AVDD) supplies by more than 2.0 V during power-down, damage can occur to the ESD structures within the analog I/Os.

## 2.2 Bring-Up Sequence

### 2.2.1 Hard Reset Signal Requirements

The hard reset signal resets all internal logic, memory elements, PLL, and the MAC core in the IXF1010/IXF1110 MAC, and is active Low. Apply the hard reset signal for a minimum period of 100 ns after the IXF1010/IXF1110 MAC have a stable power supply and CLK125, TDCLK, and CLK50 are running and stable.

In systems where the SYS\_RES pin is driven from a single board-wide reset signal, the switch or network processor only comes out of reset at the same time as the IXF1010/IXF1110 MAC, or possibly later. The TDCLK may not be applied to the IXF1010/IXF1110 MAC when the SYS\_RES pin is released. However, the system designer must ensure that the switch or network processor does not output TDCLK until it is stable and has reached its nominal operating frequency. Failure to apply a stable TDCLK to the IXF1010/IXF1110 MAC can result in the IXF1010/IXF1110 MAC training on a non-stable clock, thus causing DIP4 errors and data corruption. This requires a re-training once the TDCLK is stable.

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When the TDCLK is applied after the reset pin is released, a built-in feature in the IXF1010/IXF1110 MAC reactivates the internal reset once TDCLK is applied. The IXF1010/IXF1110 MAC extends this hardware reset internally to ensure synchronization of all internal blocks within the system. The internal reset is extended for a minimum of 4.11 ms after all clocks are stable.

**Note:** The hard reset signal needs to be applied for a minimum of 100 ns after the IXF1010/IXF1110 MAC have a stable power supply and all the input clocks are stabilized.

## 2.3 Default State of the Device

### 2.3.1 IXF1010 MAC

The following bullets describe the initial state of the IXF1010 MAC after input clocks TDCLK, CLK125, and CLK50 are applied and stable, hard reset is released, and the 4.11 ms reset recovery time has passed:

- The RGMII interface is enabled.
- The MAC is configured for 1000 Mbps full-duplex mode.
- All the ports are enabled.
- All soft reset registers are de-asserted after the system reset is de-asserted. If you wish to place a particular sub-block in reset, it must be achieved by completing a CPU access to the relevant soft reset register.
- The CPU interface can be accessed after the 4.11 ms reset recovery time has passed.
- The RX SPI4-2 is operational out of reset.
- The TX SPI4-2 is operational out of reset if TDCLK is applied and stable during reset.
- The LEDs are disabled by default.

### 2.3.2 IXF1110 MAC

The following bullets describe the initial state of the IXF1110 MAC after input clocks TDCLK, CLK125, and CLK50 are applied and stable, hard reset is released, and the 4.11 ms reset recovery time has passed:

- The SerDes interface is enabled.
- The MAC is configured for 1000 Mbps full-duplex, forced mode.
- All ports are enabled.
- All soft reset registers are de-asserted after the system reset is de-asserted. If you want to place a particular sub-block in reset, complete a CPU access to the relevant soft reset register.
- The CPU interface can be accessed after the 4.11 ms reset recovery time passes.
- The RX SPI4-2 is operational out of reset.
- The TX SPI4-2 is operational out of reset if TDCLK is applied and stable during reset.
- The LEDs are disabled by default.

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## 2.4 Device Configuration Registers

The default values for most configuration registers are appropriately set for the device to be fully operational after release of reset. However, some configuration registers may need modification to meet system requirements. Some of the registers that may need modification in any typical system deploying the IXF1010/IXF1110 MAC are listed in [Section 2.4.1](#) through [Section 2.4.8](#). These registers are the minimum configurations for the device to be up and running once reset is released.

The following registers in various blocks (for all ports) may need to be changed per system requirements. Refer to the IXF1010/IXF1110 MAC Datasheets for a detailed explanation of all registers.

### 2.4.1 Top Level Configuration Registers

- Port Enable Register (\$0x500)
  - Enables the ports for required data transfer
  - Default = ports are enabled

### 2.4.2 MAC Configuration Registers

- Station Address Register (\$Port Index + 0x00 – 0x01)
  - Sets the required station address
  - Default = Station Address 0x00
- RX Packet Filter Control Register (\$Port Index + 0x19)
  - Sets the filters on various types of packets as required (for example, VLAN, pause frames, MCAST, BCAST, UNICAST and CRC Errors) so that they are dropped in the device and not forwarded to the switch fabric.
  - Default = All VLAN, MCAST, BCAST, and UNICAST are not filtered. CRC errors and Pause frames are marked to be filtered by default and can be dropped if the appropriate bits are set in the RX FIFO Frame Drop Enable Register.
- FC Enable Register (\$Port Index + 0x12)
  - Enables IEEE 802.3 Flow Control (Pause packets)
  - Default = Flow control is enabled
- Max Frame Size Register (\$Port Index + 0x0F)
  - Sets the maximum frame size for the application
  - Default = 1518 bytes

#### 2.4.2.1 IXF1010 MAC Specific Configuration Registers

- RGMII Speed Register (\$Port Index + 0x10)
  - Sets the line RGMII speed
  - Default = 1000 Mbps full-duplex
- Diverse Configuration Write Register (\$Port Index + 0x18)
  - Sets the various configurations such as TX CRC appending and packet padding.
  - Default = packet padding and TX CRC appending are disabled

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### 2.4.2.2 IXF1110 MAC Specific Configuration Registers

- Diverse Configuration Write Register (\$Port Index + 0x18)
  - Sets the various configurations (for example, TX CRC appending and packet padding)
  - Sets the mode to forced mode or auto-negotiation mode
  - Default = Forced mode operation, packet padding and TX CRC appending are disabled

### 2.4.3 Transmit FIFO Configuration Registers

- High Watermark Register – \$0x600 - 0x609
  - Sets the per-port High Watermark for SPI4-2 back pressure. When the amount of data in the TX FIFO crosses this setting, the SPI4-2 FIFO status changes from HUNGRY to SATISFIED.
  - Default = 1584 bytes
- Low Watermark Register – \$0x60A- 0x613
  - Sets the per-port Low Watermark for SPI4-2 back pressure. When the amount of data in the TX FIFO is below this watermark, the SPI4-2 TX FIFO status for the port is STARVING. If the amount of data is above the Low watermark but below the High Watermark, SPI4-2 TX FIFO status is HUNGRY.
  - Default = 464 bytes
- MAC Transfer Threshold Register – \$0x614- 0x61D
  - Sets the threshold at which the FIFO begins to transfer data to the MAC.
  - Default = 256 bytes

### 2.4.4 Receive FIFO Configuration Registers

- High Watermark Register – \$0x580 - 0x589
  - Sets the per-port High Watermark at the point a flow control request (Xoff) is sent to the link partner.
  - Default = 1856 bytes
- Low Watermark Register – \$0x58A- 0x593
  - Sets the per-port Low Watermark at the point a flow control request with time value = 0 (Xon) is sent to the link partner.
  - Default = 1840 bytes
- RX FIFO Errored Frame Drop Enable Register – \$0x59F (for all ports)
  - Determines whether filtered packets are forwarded to the SPI4-2 interface or dropped in the RX FIFO
  - Default = All filtered packets are passed to the SPI4-2 interface and not dropped in the RX FIFO.

### 2.4.5 LED Block Configuration Registers

- LED Control Register (\$0x509)

- Sets the LED mode (See the IXF1010/IXF1110 MAC Datasheets for further information)
- Enables the LED outputs.
- Default = LEDs are disabled and Mode 0 operation.
- Link LED Enable Register (\$0x502)
  - Programmed by system software to reflect the link status of the MAC to enable the per port RX LED green-on state.
  - Default = Link LED bits are set to zero, disabling the RX LED green-on state.

## 2.4.6 SPI4-2 Block Configuration Registers

### 2.4.6.1 SPI4-2 Initialization

The following is a list of SPI4-2 parameters, which must be programmed to match the application for proper operation of the IXF1010/IXF1110 MAC SPI4-2 interface.

#### 2.4.6.1.1 CALENDAR\_LEN

CALENDAR\_LEN specifies the length of each calendar sequence. The IXF1010/IXF1110 MAC are 10-port devices. Therefore, CALENDAR\_LEN is fixed at 10 for both TX and RX data paths.

#### 2.4.6.1.2 CALENDAR\_M

CALENDAR\_M specifies the number of times the calendar port status sequence is repeated between the framing and DIP2 cycle of the calendar sequence. In the IXF1010/IXF1110 MAC, the TX path CALENDAR\_M is fixed at 1. Thus, the port status for ports 0 - 9 will be transmitted only once between the framing and DIP2 cycle of the calendar sequence. In the IXF1110 MAC, the RX path CALENDAR\_M is also fixed at 1. Thus, the status for port 0-9 must only be sent once between framing and DIP2. Therefore, the value of both TX and RX CALENDAR\_M parameters is always fixed at 1.

#### 2.4.6.1.3 DIP2\_Thr

DIP2\_Thr is a parameter specifying the number of consecutive correct DIP2s required by the RX SPI4-2 to validate a calendar sequence and terminate transmission of training sequences. In the SPI4-2 RX Calendar Register (\$0x702), bits 19:16 specify this parameter. The default value for DIP2\_Thr is 1.

#### 2.4.6.1.4 Loss\_of\_Sync

Loss\_of\_Sync is a parameter specifying the number of consecutive framing calendar cycles required to indicate a loss of synchronization and restart transmission of training sequences. SPI4-2 RX Calendar Register (\$0x702) bits 11:8 specify this parameter. The default value for Loss\_of\_Sync is 3.

#### 2.4.6.1.5 DATA\_MAX\_T

DATA\_MAX\_T is an RX SPI4-2 parameter specifying the interval between transmission of periodic training sequences. SPI4-2 RX Training Register (\$0x701) bits 15:0 specify this parameter. The default value for DATA\_MAX\_T is 0x0000, which disables periodic training sequence transmission. This may vary per implementation.

#### 2.4.6.1.6 REP\_T

REP\_T is an RX SPI4-2 parameter specifying the number of training sequence repetitions to be scheduled every DATA\_MAX\_T interval. SPI4-2 RX Training Register (\$0x701) bits 23:16 specify this parameter. The default value for REP\_T is 0x00.

#### 2.4.6.1.7 DIP4\_UnLock

DIP4\_UnLock is a TX SPI4-2 parameter specifying the number of consecutive incorrect DIP4 fields to be detected to declare loss of synchronization and drive TSTAT[1:0] bus with framing. SPI4-2 TX Synchronization Register (\$0x703) bits 15:8 specify this parameter. The default value for DIP4\_UnLock is 0x04.

#### 2.4.6.1.8 DIP4\_Lock

DIP4\_Lock is a TX SPI4-2 parameter specifying the number of consecutive correct DIP4 fields to be detected to declare synchronization achieved and enable the calendar sequence. SPI4-2 TX Synchronization Register (\$0x703) bits 7:0 specify this parameter. The default value for DIP4\_Lock is 0x20.

#### 2.4.6.1.9 MaxBurst1

MaxBurst1 is an RX SPI4-2 parameter specifying the maximum number of 16-byte blocks that may be transmitted when the RX FIFO status indicates STARVING. SPI4-2 RX Burst Size Register (\$0:x700) bits 24:16 specify this parameter. The default value for MaxBurst1 is 0x006, indicating a MaxBurst1 of 96 bytes.

#### 2.4.6.1.10 MaxBurst2

MaxBurst2 is an RX SPI4-2 parameter specifying the maximum number of 16-byte blocks that may be transmitted when the RX FIFO status indicates HUNGRY. SPI4-2 RX Burst Size Register (\$0x700) bits 8:0 specify this parameter. The default value for MaxBurst2 is 0x002, indicating a MaxBurst2 of 32 bytes.

#### 2.4.6.1.11 RSCLK\_invert

RSCLK\_invert is an RX SPI4-2 parameter that determines if the RX FIFO status is captured on the rising or falling edge of RSCLK. The default for this bit is 0, indicating that the RX FIFO status is captured on the rising edge of RSCLK.

#### 2.4.6.1.12 TSCLK\_invert

TSCLK\_invert is a TX SPI4-2 parameter that determines if the IXF1010 MAC and IXF1110 MAC TX FIFO status is launched on the rising or falling edge of the TSCLK output. The default value for this bit is 0, indicating that the TX FIFO status is launched on the rising edge of TSCLK.

### 2.4.6.2 SPI4-2 Training

The IXF1010/IXF1110 MAC Dynamic Phase Alignment (DPA) feature requires a SPI4-2 training pattern on startup.

**Note:** The IXF1010/IXF1110 MAC will not initialize the SPI4-2 interface when the upstream SPI4-2 device fails to provide the training pattern.

The SPI4-2 RX Calendar Register (\$0x702) bits 13:12 indicate when training is achieved and that the device is ready for data transmission and reception on the SPI4-2 interface as follows:

1. The RX SPI4-2 Sync (bit 13) indicates that training is completed on the RX SPI4-2. When bit 13 = 1, the RX SPI4-2 has sent training patterns and received a valid 10-port calendar from the upstream SPI4-2 device.
2. The TX SPI4-2 Sync (bit 12) indicates that the IXF1010/IXF1110 MAC has received valid training patterns and have successfully trained with the upstream SPI4-2 device. When bit 12 = 1, the IXF1010/IXF1110 MAC has initiated a 10-port calendar on TSTAT.

## 2.4.7 IXF1110 MAC Auto-Negotiation and Link Establishment

In SerDes mode, the IXF1110 MAC must be establish a link with the link partner before data can be transferred across the device. The TX FIFO is disabled until a valid link is established in auto-negotiation or forced mode. The TX FIFO asserts back-pressure to the switch fabric by signaling SATISFIED for the port until a link-up is complete. [Section 2.4.7.1](#) and [Section 2.4.7.2](#) explain how to detect when a valid link is established between the IXF1110 MAC and the fiber link partner.

**Note:** The default state at power-up or out of reset is a forced-mode operation.

### 2.4.7.1 Auto-Negotiation Mode

Auto-negotiation is carried out by an internal state machine within the MAC in the IXF1110 MAC. The IXF1110 MAC complies with the IEEE 802.3z standard.

The following three registers perform various auto-negotiation processes:

- RX Config Word Register ( $\$Port\_Index + 0x16$ ): Auto-negotiation base page ability
- TX Config Word Register ( $\$Port\_Index + 0x17$ ): Auto-negotiation advertisement
- Diverse Config Register ( $\$Port\_Index + 0x18$ ): Enables auto-negotiation

The TX Config Word Register ( $\$Port\_Index + 0x17$ ) must be written to program the modes advertised. The Diverse Config Register ( $\$Port\_Index + 0x18$ ) bit 5 (AN\_enable) must be written to enable auto-negotiation. The RX Config Word Register ( $\$Port\_Index + 0x16$ ) bit 21 (AN\_complete) must be polled to determine when auto-negotiation is complete and is used to determine the link partners capabilities. The following MAC registers must be programmed to match the results upon completion:

- **Link LED:** Link LED Enable Register ( $\$0x502$ )
- **Flow Control Enable Register:** If the RX Config Word register indicates the link partner does not support flow control, the FC Enable Register ( $\$Port\_Index + 0x12$ ) must be updated to reflect this change [see FC Enable Register ( $\$Port\_Index + 0x12$ )].

A valid link is established when the (AN\_complete) bit is set and the RX\_Sync bit reports synchronization has occurred. Both register bits are located in the RX Config Word Register ( $\$Port\_Index + 0x16$ ).

RX\_Sync indicates that a loss of synchronization occurred if link goes down after auto-negotiation is completed. The IXF1010 MAC restarts auto-negotiation and attempts to reestablish a link. The AN\_complete but is set and the RX\_sync bit shows that synchronization has occurred once a link is reestablished.

Bit 5 of the Diverse Config Register (AN\_enable) must be de-asserted, then re-asserted, to manually restart auto-negotiation.

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### 2.4.7.2 Forced Mode Link Determination

When the IXF1110 MAC is in forced mode operation, the RX Config Word Register (\$Port\_Index + 0x16) bit 20 RX\_Sync indicates when synchronization has occurred and valid link is established. Once a link is established, the Link LED Enable register must be updated by the system software to reflect the change in link status.

The RX\_Sync bit indicates a loss of synchronization when link is down.

### 2.4.8 IXF1010 MAC Link Establishment

Link is determined by the PHY in copper applications using the IXF1010 MAC. The system software must read the PHY status register to determine when link is established and ensure the IXF1010 MAC matches the PHY speed and duplex. After the PHY completes auto-negotiation, the IXF1010 MAC reads the PHY Auto-Negotiation Link Partner Base Page Ability Register. From the settings in this register, the following IXF1010 MAC registers must be programmed to match the connected PHY configuration:

- **Speed:** The IXF1010 MAC speed is set to either 100 Mbps or 1000 Mbps in the RGMII Speed Register (\$Port Index + 0x10).
- **Link:** While link is established, write to the Link LED Enable Register (\$0x502) (link to register). This register controls link LED, which does not update automatically. Update the Link LED Register when there is a change in link status so that the link LED green shows expected behavior.
- **Flow Control:** The FC Enable Register (\$Port Index + 0x12) must be updated to reflect this change if the link partner does not support flow control.

**Note:** Update the IXF1010 MAC registers if any changes are detected in the link partner speed, duplex, or flow control capabilities.

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## 3.0 Guidelines for Configuration Changes

Section 3.0 provides recommendations on the steps to be followed during configuration changes.

**Note:** Cortina recommends that configuration changes not be performed during packet transfers. Such “on-the-fly” configuration changes are not supported and will lead to unpredictable misbehavior of the device for a certain duration after the configuration change is made.

### 3.1 Top Level Configurations

Port Enable Register

- Port enable assertion must be done when data transfer is not in progress in receive and transmit paths.

#### 3.1.1 MAC Configurations

##### 3.1.1.1 IXF1010 MAC

- RGMII speed mode:
  - This register must be changed only when packet transfer is not underway and must always be programmed to match the PHY configuration.
- The following configurations must not be changed when packet transfer is underway. Device misbehavior may occur if performed.
  - IPG Timers
  - Pause Threshold Value
  - Short/Runts Threshold
  - CRC Appending
  - Padding Enable
  - MaxFramesize
  - FC Enable.

##### 3.1.1.2 IXF1110 MAC

Auto-negotiation mode or forced mode must not be changed while data is being transmitted. Changing the mode will cause the link to go down, which will corrupt any transfers currently occurring on the SerDes interface.

The following configurations must not be changed when packet transfer is underway. Device misbehavior may occur if performed:

- IPG timers
- Pause Threshold Value
- Short/Runts Threshold
- CRC Appending
- Padding Enable

- 
- MaxFramesize
  - FC Enable

### **3.1.2 Transmit FIFO Configurations**

The following values must not be changed when data transfer is underway:

- High Watermark Register
- Low Watermark Register
- MAC Threshold Register

### **3.1.3 Receive FIFO Configurations**

The following values must not be changed when data transfer is underway:

- High Watermark Register
- Low Watermark Register

### **3.1.4 SPI4-2 Block Configurations**

The following SPI4-2 parameters should not be changed during packet transfer:

- MAXBURST1
- MAXBURST2

Cortina recommends that the following parameters be changed only before the RSCLK is applied:

- RSCLK\_invert
- DIP2\_Thr
- Loss\_Of\_Sync

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## 4.0 Initialization Summary

In summary, power sequences and hard reset requirements must be followed for proper IXF1010/IXF1110 MAC operation. At this point, the various registers can be modified if the default configuration requires a change to match the application.

**Note:** Take care when changing certain configuration registers as stated in [Section 3.0, Guidelines for Configuration Changes](#), on page 13.



**For additional product and ordering information:**

[www.cortina-systems.com](http://www.cortina-systems.com)